application note

TAU-TRON INC., A UNIT OF GENERAL SIGNAL
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AN-1
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DS3 JITTER MEASUREMENTS WITH THE S5200D

Jitter in digital communication systems is a key parameter that can affect performance if not properly controlled. High capacity, multiple section, multiplexed systems and digital switching systems are particularly sensitive to jitter. The S5200D provides a jitter monitor voltage output that weights the spectral components of jitter according to their potential effect on system performance. This voltage can be monitored with a simple ac voltmeter to provide an easy, yet effective way, to characterize systems jitter. The monitor point can also be used for more detailed analysis of jitter and is applicable to both in-service and off-line applications.

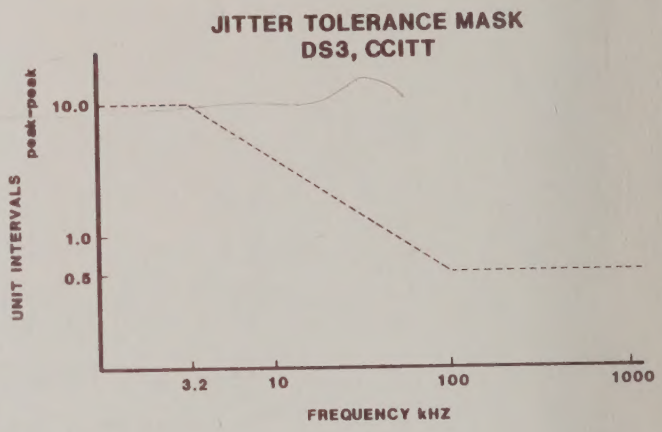
GENERAL

Jitter in a digital communication system is a key parameter that must be properly controlled. This is particularly true in multiplexed systems with a number of tandem regenerators since each regenerator and multiplex process can modify and even increase signal jitter. Too much jitter can cause timing recovery loops to lose lock and multiplexers to buffer stuffing and synchronization problems. Switched digital systems also fare better when jitter is within controlled limits.

Jitter, or phase perturbations of the incoming or outgoing bit stream, exists for many reasons. Sensitivity to bit pattern variations, phase noise of system oscillators, system response non-linearities, timing loop response, multiplexing techniques and the compounding effects of tandem hops all affect jitter. System designers pay close attention to these parameters since they can be critical to solid performance.

JITTER SPECIFICATIONS

System jitter, generally, is not easily defined because of the statistical nature of its origin. System designers commonly define masks, however, specifying the tolerance level in bits or unit intervals of jitter that a system should have at a particular frequency. As an example, the CCITT mask for DS3 rates is shown below.

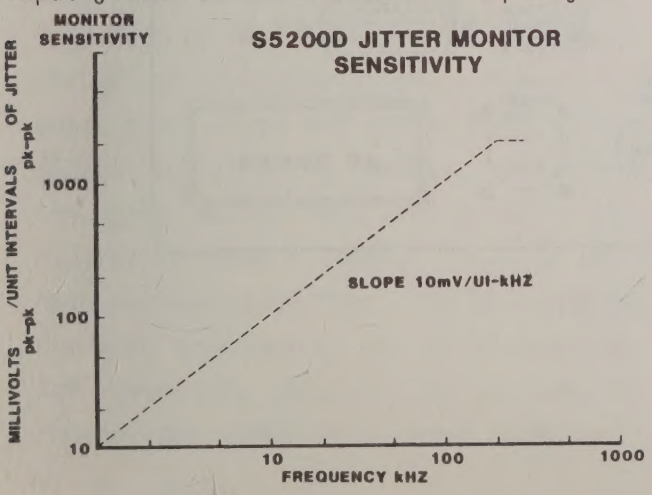


It is also common to specify a system jitter transfer function. This usually requires that the input jitter not be increased, or be increased only slightly, after passing through a particular system section. The general shape of the jitter tolerance mask also pertains to the output jitter of many systems. Low frequency jitter often caused by multiplexer waiting time is usally larger but systems can tolerate higher jitter levels at low frequencies. Higher frequency jitter is usually less since it does not propogate through narrower timing recovery loops and systems cannot tolerate as much of this high frequency jitter.

S5200D JITTER OUTPUT

The S5200D uses a combination frequency-phase locked loop to optimize parameters for transmission test and measurement applications. Because of the separation of frequency and phase functions the acquisition behavior and phase response can be designed nearly independently to achieve fast acquisition, tolerance-to-phase jitter ability to handle periods of data interruptions or inactivity, and to process non-ideal waveforms to assure reliable and accurate measurements.

A buffered frequency-phase loop control voltage is available at the S5200D Receiver Monitor connector. This voltage provides a frequency weighted output proportional to the amount of jitter present at the Receiver DS3 input as shown in the following figure. This curve shows the monitor voltage output sensitivity to input jitter as a function of frequency.



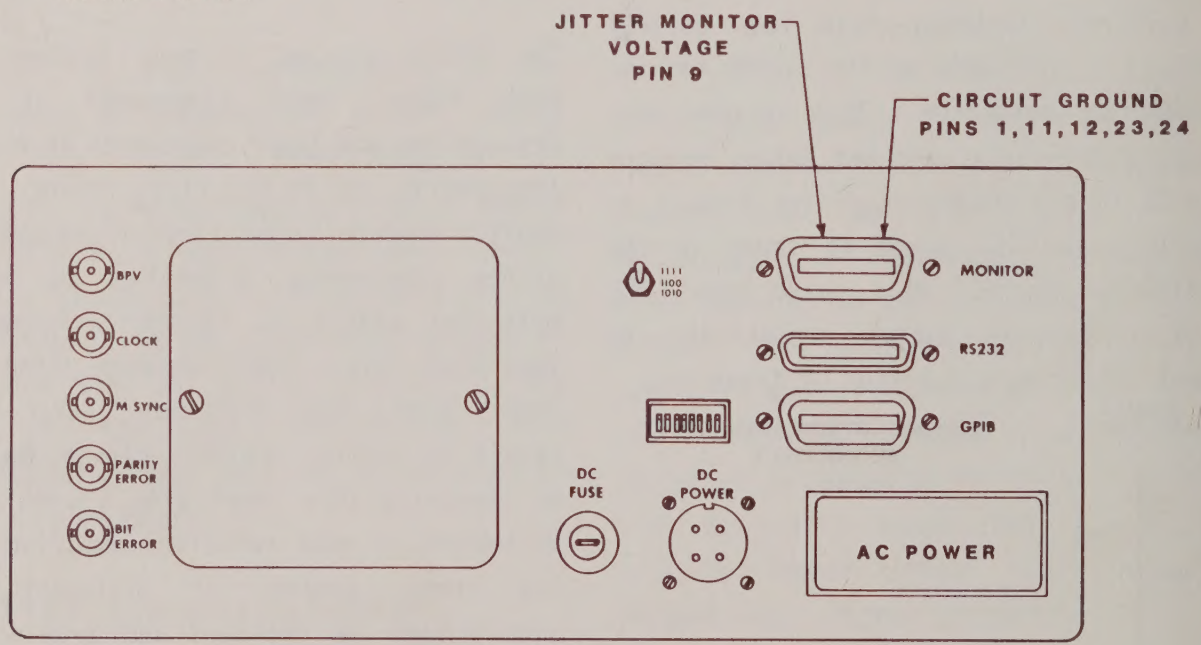
The monitor voltage will follow the frequency of the input jitter, however, the voltage level is weighted so that high amounts of jitter at low frequencies and low amounts of jitter at higher frequencies will result in a similar absolute monitor voltage level. For example, a DS3 signal with 5-unit intervals (UIp-p) of peak-to-peak jitter at 1 kHz will result in a 1-kHz monitor voltage with a 10mVp-p-/UIp-p x 5 = 50mVp-p monitor voltage level. 0.5 unit intervals of jitter at 10 kHz will also result in a 50mVp-p monitor voltage level.

The jitter present in many systems may have higher level components at low frequencies and lower components at higher frequencies, as in the first figure. The monitor voltage output tends to weight the jitter components according to their potential effect on system performance. Thus high level, low frequency jitter or lower level, high frequency jitter will result in similar monitor voltage levels. By measuring this level with a simple ac voltmeter, a good relative comparison of the jitter content of different DS3 signals can be obtained and provide an effective, yet simple way to characterize overall system jitter. The jitter monitor voltage is on pin 9 of the 24-pin rear panel monitor connector and circuit ground is on pins 1, 11, 12, 23 and 24.

SUMMARY

For field use the S5200D and a simple ac voltmeter can provide a relative comparison of the amount of jitter present on the DS3 signals within systems and can be useful in trouble shooting. A chart recorder can also be used to monitor longer term jitter fluctuations. Jitter could be analyzed in greater detail, in the laboratory for example, by observing the monitor voltage with a spectrum analyzer or frequency selective voltmeter to discern not only level but frequency content. This access point to the jitter on a DS3 signal is available when the S5200D is used for in-service monitor point measurement or in off-line testing.

S5200D RECEIVER REAR-PANEL



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TWO WAY RS-449 (RS-422) OR RS-232C CAPABILITY FOR THE S5200D RECEIVER

(FOR REMOTE DS3 MONITORING AND CONTROL OVER LOW SPEED SERIAL COMMUNICATIONS LINKS)

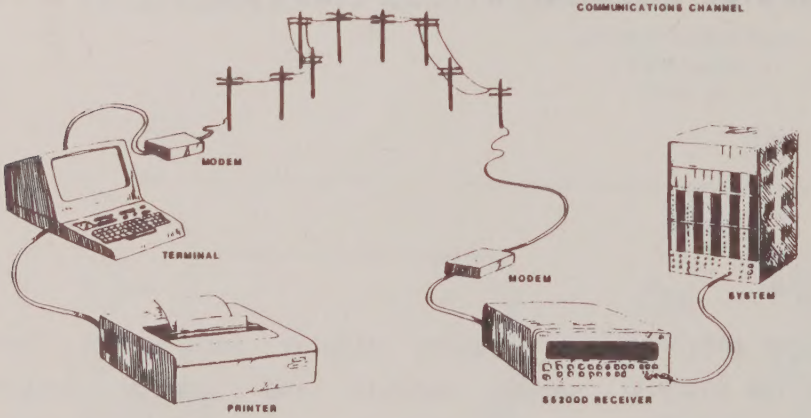
The S5200D DS3 Receiver has been enhanced to provide remote control via the RS-232C interface or RS-449 (with balanced RS-422 electrical characteristics). All of the measurement power and capabilities of the S5200D installed at remote, unattended locations cannot only be accessed but controlled from a central location with this two-way capability. ASCII formatted commands from nearly any RS-232C or RS-449 compatible terminal can be used to control the S5200D measurement modes and to request display information, error second outputs and summary outputs. Remote commands correspond to the S5200D front panel so interfacing with the S5200D by a remote link is almost like operating the unit directly. The S5200D serial interface can be used with modems or low speed data interfaces to achieve user friendly remote system monitoring and diagnostics capabilities of DS3 compatible systems.

REMOTE CONTROL APPLICATIONS

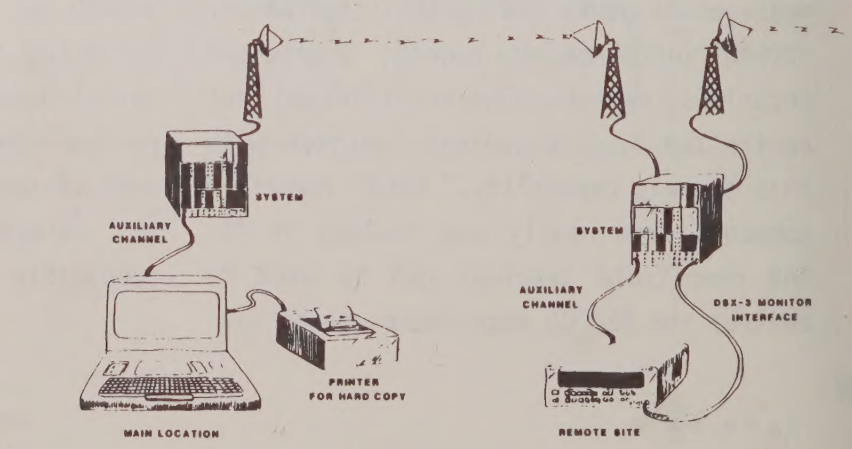
A low cost video display terminal or teletype terminal and a low speed asynchronous data channel are all that is required in the central office or monitoring location to access the remote test sets. Inexpensive modem interfaces and existing telephone lines or an auxiliary data channel available in many high capacity communications systems could provide the serial communication link as shown in the figures below.

Dial-up modems could also be used which would permit any one of many remote S5200D systems to be accessed by a single terminal in the central office. For example, S5200D receivers could be connected to the low level DS3 monitor point of a number of microwave or light guide stations. Each S5200D could then be dialed up and requested to provide system summary status collected over a past interval or could be requested to provide current performance information.

S5200D REMOTE SYSTEM MONITORING
THRU SEPARATE LOW SPEED COMMUNICATIONS CHANNEL

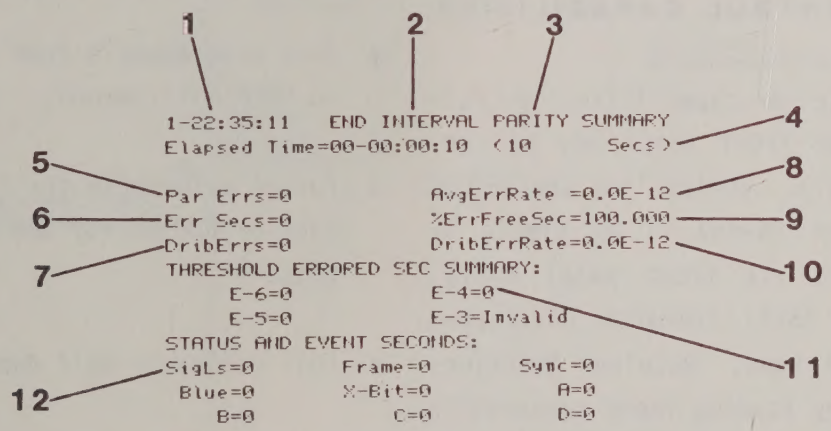


S5200D REMOTE SYSTEM MONITORING
THRU SYSTEM AUXILIARY CHANNEL



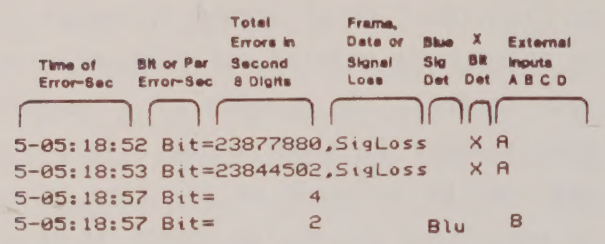
REMOTE DATA ACQUISITION

Locally displayed measurements and status may be requested by remote commands and output to the central controller. One command accesses DS3 signal status (frame loss, signal loss, etc.) while another accesses the test set measurement mode. Another command "snapshots" the current 40-character S5200D display. Since all S5200D measurements can be selected and displayed by remote control, all measurement capabilities are available to a remote controller. In addition, the normal printer output functions available locally such as a complete measurement summary or individual error second printouts may be selectively enabled and disabled by remote control. An example of a measurement summary is shown below. This summary can be accessed at any time or can be controlled to provide status at selected intervals.



1. Time of day when summary was formatted: day of week, hour, minutes, seconds.
2. Summary type: End of Interval or Immediate summary.
3. Measurement type bit or parity.
4. Elapsed time: days-hours, minutes, seconds and total seconds.
5. Total errors since start of elapsed interval.
6. Total error-seconds since start of elapsed interval.
7. Total dribbling errors since start of elapsed interval.
8. Average error-rate.
9. % error-free seconds.
10. Dribbling error-rate.
11. Threshold error-seconds: number of error-seconds during which the error-rate exceeded 10^{-6}, 10^{-5}, 10^{-4}, or 10^{-3}.
12. Status and event seconds: number of seconds during which any of the listed events were detected.

An example of several error second printouts is shown below:


Time of Error-Sec
BR or Par Error-Sec
Total Errors in Second 8 Digits
Frame, Data or Signal Loss
Blue Sig Det
X BR Det
External Inputs A B C D
5-05:18:52 Bit=23877880,SigLoss X A
5-05:18:53 Bit=23844502,SigLoss X A
5-05:18:57 Bit= 4
5-05:18:57 Bit= 2 Blu B

REMOTE CONTROL CAPABILITIES

All S5200D Receiver capabilities controllable from the front panel may be controlled remotely. Controlling the S5200D via RS-232C or RS-449 is as simple as controlling it via front panel entry. Two-character ASCII commands correspond to front panel keys. Receiver functions are selected by issuing these commands in the same sequence as front panel key/hits. Five additional commands are provided to acquire measurements or status from the Receiver, enable/disable (lockout) the front panel, and reinitialize the S5200D to its power up state. There is also an output indication of improper commands.

OTHER S5200D INTERFACES

In addition to these serial interfaces for the S5200D Receiver, IEEE-488 GPIB interface is also available for both Receiver and Transmitter.

SERIAL DATA INTERFACE

- EIA Standard RS-449 and EIA Standard RS-422 or EIA Standard RS-232C.
- Rate programmable from 110 bits/second to 9600 bits/second.
- Format selectable for 7 or 8 data bits, even or odd parity and 1 or 2 stop bits.
- Full duplex or half duplex modes.

The S5200D Receiver two-way RS-449 (RS-422) or RS-232C capability interface can be ordered or more information can be obtained on this or the IEEE-488 Interface, by contacting the Tau-Tron Sales Department at (617) 256-9013.

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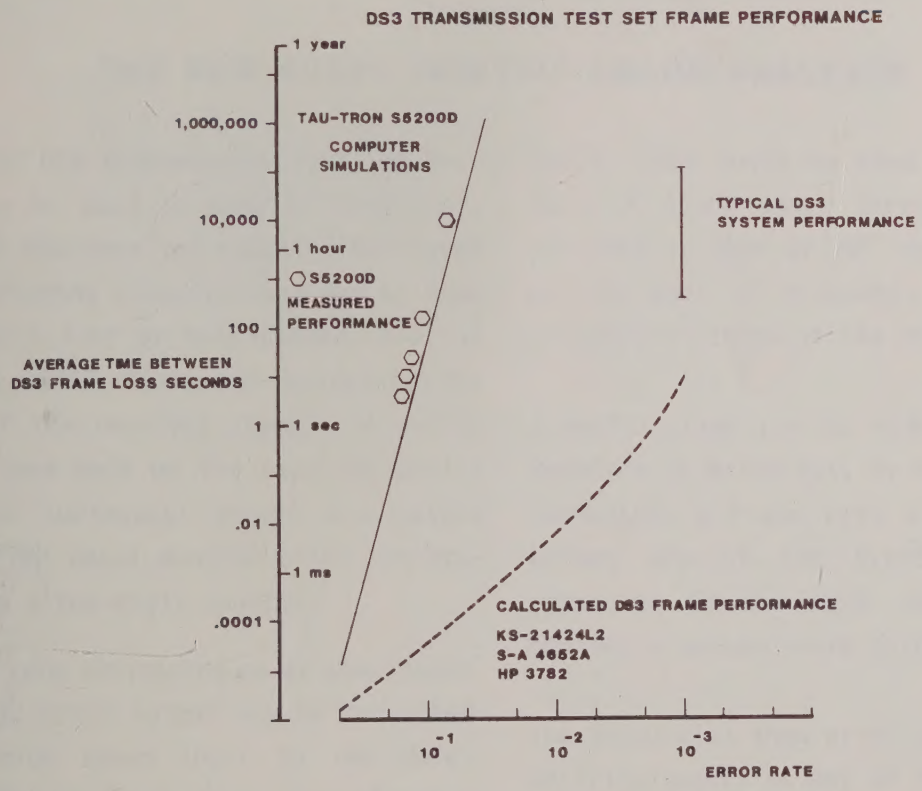
AN-3
December 1982

IS YOUR TRANSMISSION SYSTEM THIS GOOD?



A DS3 transmission test capable of providing accurate measurements should achieve fast acquisition and maintain frame synchronization under high error conditions; otherwise, the test set may indicate system performance worse than the actual performance and efforts to verify performance or isolate problems could be frustrated.

The DS3 frame circuitry of the Tau-Tron S5200D receiver has been optimized to provide the performance needed for accurate DS3 monitoring and diagnostic applications.

The figure above shows the average time between DS3 frame loss versus error rate for the Tau-Tron S5200D and other equipment. The Tau-Tron S5200D system is superior to other DS3 test equipment and exceeds the performance of most systems so you can be confident that system measurements using the S5200D are a true indication of system performance.

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ENHANCING THE S5200C WITH THE NEW MODEL PRINTING ERROR ANALYZER

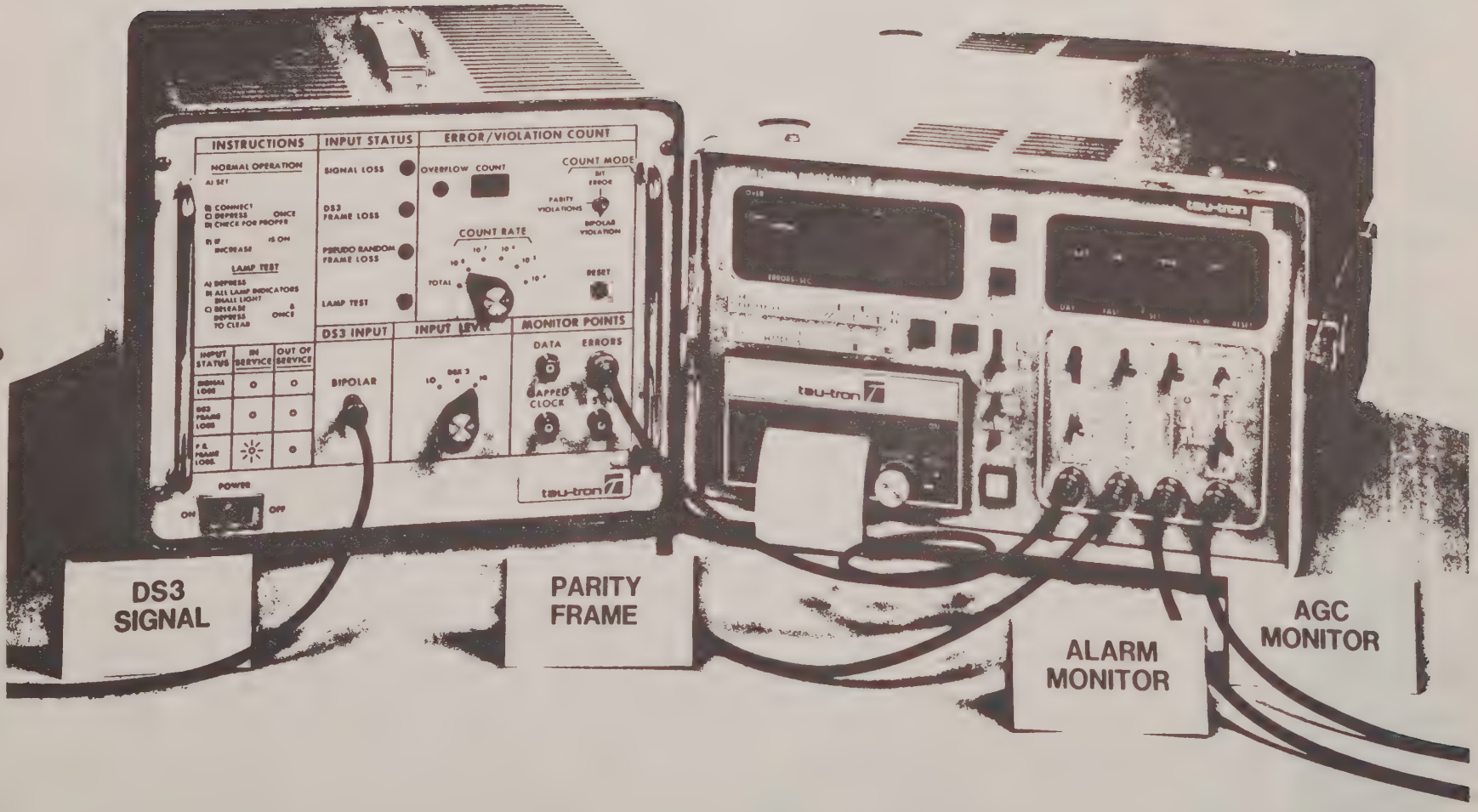
The S5200C DS3 Transmission Test Set Receiver may be used to monitor live traffic. The DS3 Receiver contains Bell-compatible framing circuitry and may be used to bridge a line or multiplexer, and, as a result, will frame and calculate the parity of the received signal. A parity test is then made on the received parity bits, and subsequent errors are output from a front panel monitor point and displayed on a two-digit counter.

For long term monitoring on an unattended basis, the error output may be connected as the high speed input to the Model S5000 Printing Error Analyzer. The occurrence of a parity error pulse will cause the Printing Error Analyzer to print that error information along with the time-of-day and the condition of the three other S5000 inputs.

An analog input can accept a ±20V or ±200V signal. In a radio system, for example, this could be used to monitor the AGC. A front panel threshold adjust is provided so that an AGC voltage limit can be set and, if exceeded, would cause a triggering action of the printer.

A modification can be made to the S5200C Receiver to bring out, by a rear panel BNC connector, a Frame Loss signal which may become one of the Event Inputs. The remaining Event Input can be used to monitor a system alarm point.

The S5000 will then print out whenever any activity occurs on any of the four inputs. The printout would include time-of-day, total errors during a 1-second interval triggered by any of the four inputs, the level of the analog input and the status of the event inputs. A periodic mode can also be programmed whereby every 1 minute, 15 minutes, 1 hour, or 24 hours a summary of the preceding periods will be printed.


INSTRUCTIONS
INPUT STATUS
ERROR/VIOLATION COUNT
NORMAL OPERATION
LAMP TEST
SIGNAL LOSS
DS3 FRAME LOSS
PSEUDO RANDOM FRAME LOSS
LAMP TEST
OVERFLOW COUNT
COUNT MODE
PARITY VIOLATIONS
BIPOLAR VIOLATION
COUNT RATE
TOTAL
RESET
DS3 INPUT
INPUT LEVEL
MONITOR POINTS
DATA
ERRORS
BIPOLAR
CLOCK
INPUT STATUS
IN SERVICE
OUT OF SERVICE
POWER
ON
OFF
tau-tron
DS3 SIGNAL
PARITY FRAME
ALARM MONITOR
AGC MONITOR

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AN-5
March 1983

PSUEDORANDOM SEQUENCES

Psuedorandom binary sequences are now playing an important role in information security, communications and digital testing, radar and ranging systems, and the simulation of random events. These sequences have properties which closely approximate true randomness, and they can easily be generated with low cost shift registers. New application areas are constantly being discovered.

THE PROPERTIES OF RANDOMNESS

Randomness is a measure of the unpredictability of an event, and the term random refers more to the method of selection rather than to the chosen pattern itself. Any defined selection method can never be truly random -- hence the name pseudo-random. For example, let's consider the basic properties of a random sequence generated by tossing an unbiased coin and recording the results. Probability theory says that the resulting sequence should have three important properties:

1. The number of heads is approximately equal to the number of tails.

2. The number of runs (of consecutive heads or tails) of length n is about twice the number of runs of length n + 1; i.e., one-half the runs are of length one, one-fourth of length two, one-eight of length three, etc.

3. The autocorrelation of the sequence has a peak at the origin and decreases rapidly away from it. Here, the auto correlation of a periodic finite sequence is defined as:

$$C(T) = \frac{1}{P} \sum_{n=1}^{P} A_n A_{n+T}$$

Where A_n = +1 for heads, -1 for tails and P = the period of sequence (or length).

Patterns possessing these same properties of randomness can be produced by various

methods. Some systems are based on true random generators like radioactive decay or shot noise from a zener diode, and certain computer programs have been written to select random numbers. For example, squaring a twelve-digit number and keeping the middle twelve digits will yield a pseudorandom sequence. Unfortunately, these methods are generally expensive and not reproducible.

SHIFT REGISTER GENERATORS

The shift register generator has none of these shortcomings. Binary sequences of 1's and 0's are easily generated, and, although the patterns fulfill the conditions of randomness, they are predictable. This predictability feature of shift register generators opens up a myriad of applications, including message scramblers and bit-error rate testers.

A pseudorandom binary sequence generator produces a cyclic sequence of pseudorandom 1's and 0's. The heart of the generator is the feedback shift register. A basic shift register is just a string of cascaded flip-flops. On a clock signal, an input value is accepted into the first stage, and with each successive clock pulse these input data are shifted through the register's successive stages. If no new data are entered into stage one, the clock signals will eventually clear the register. A sequence generator is made by feeding data back from some of the stages to the input of the first stage. Feedback from various stages is generally added, modulo-2, by an exclusive-OR gate. A sequence generator using this modulo-2 addition is called linear. The last stage of the register is usually added together and fed into stage one, so it can be seen that the sequence is determined by the number of stages in the register plus the feedback taps used. The sequence produced fulfills the conditions for randomness, yet it is a repeating pattern. The number of bits in the pattern is also determined by the number of stages in the register and the feedback connections used. Certain combinations of feedback taps produce the longest non-repeating sequence possible for a given number of shift register stages; this sequence is called a maximal length or m-sequence.

With a shift register containing n stages, the maximum number of binary states possible to produce maximal length sequences is 2^n. The all-zero condition must be prevented because two zeros undergoing modulo-2 addition yield zero; this would feed a zero into stage one -- the resulting sequence would be a useless series of all 0's. Therefore, with the all-zero pattern in the shift register restricted, the maximal length pseudorandom pattern will contain 2^n-1 bits. In Figure 1, a five-stage shift register generator is illustrated along with the

	GENERATED SEQUENCE				
	1	2	3	4	5
1	1	1	1	1	1
2	0	1	1	1	1
3	1	0	1	1	1
4	0	1	0	1	1
5	0	0	1	0	1
6	0	0	0	1	0
7	1	0	0	0	1
8	0	1	0	0	0
9	0	0	1	0	0
10	1	0	0	1	0
11	0	1	0	0	1
12	1	0	1	0	0
13	0	1	0	1	0
14	1	0	1	0	1
15	1	1	0	1	0
16	0	1	1	0	1
17	0	0	1	1	0
18	0	0	0	1	1
19	0	0	0	0	1
20	1	0	0	0	0
21	1	1	0	0	0
22	1	1	1	0	0
23	0	1	1	1	0
24	0	0	1	1	1
25	1	0	0	1	1
26	1	1	0	0	1
27	0	1	1	0	0
28	1	0	1	1	0
29	1	1	0	1	1
30	1	1	1	0	1
31	1	1	1	1	0
1	1	1	1	1	1

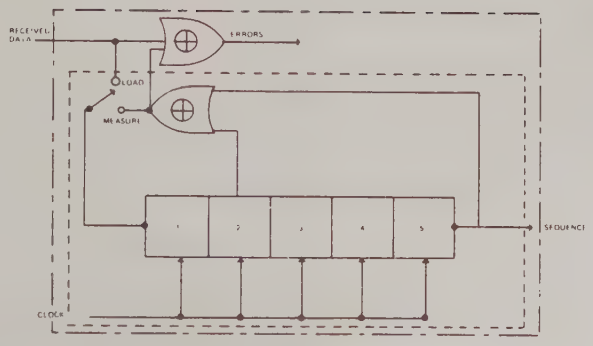

Figure 1

NUMBER OF STAGES	TAPS	REVERSE TAPS	SEQUENCE LENGTH (IN BITS)
3	2, 3	1, 3	7
4	3, 4	1, 4	15
5	3, 5	2, 5	31
6	5, 6	1, 6	63
7	6, 7	1, 7	127
8	2, 3, 4, 8	4, 5, 6, 8	255
9	5, 9	4, 9	511
10	7, 10	3, 10	1023

Figure 2

pseudorandom sequence produced. The sequence may be picked up at any of the register stages, shifted by one bit per stage.

One interesting property of shift register sequences is reverse sequence. A reversed bit pattern may be obtained by altering the feedback taps. A list of some of the taps for m-sequences and the reverse taps is shown in Figure 2. It can be seen from the list that taps taken at stages 3 and 4, for a four-stage shift register, will produce a forward pattern, and the taps taken at stages 1 and 4 will yield its reverse pattern.

As the number of stages in the shift register is increased, the number of possible maximal length sequences also increases. For a shift register of length four, there are only two possible m-sequences, but for a shift register of length 16, the number of m-sequences increases to 2040.

If the feedback circuit uses some other operation besides modulo-2 addition or if some other taps are used, the sequence will be a shorter nonlinear sequence. This opens up the possibility of generating an almost infinite variety of codes and code lengths.

PROPERTIES OF MAXIMAL LINEAR SEQUENCES

To show that the three properties of randomness hold true for maximal linear sequences, the shift register goes through every possible state except all zeros. First, there will be 2^n-1 ones

and $2^{n-1}-1$ zeros in the sequence, where n is the length of the register. Here, the first property holds true since the number of zeros is approximately equal to the number of ones. In order to find out how many runs of ones of length k occur, the following should be considered; n consecutive terms beginning with zero, then k ones, zero, and finally n-k-2 terms. For $0<k<n-1$, the occurrence would be 2^{n-k-2}. This would also be true for runs of zeros. Thus, the second property holds true for the autocorrelation, $\{A_n\}$ must be transformed into $\{B_n = 1-2a_n\}$ by replacing the zeros with ones and the ones with minus ones. Modulo-2 addition transforms into multiplication, which means $\{A_k\} \oplus \{A_{k+m}\} = \{A_{k+n}\}$ implies $\{B_k\} \times \{B_{k+m}\} = \{B_{k+n}\}$. Thus, the autocorrelation of

$$C(T) = \frac{1}{2^n-1} \sum_{k=1}^{2^n-1} b_k\, b_k + T$$

$$= \frac{1}{2^n-1} \sum_{k=1}^{2^n-1} b_k + n \text{ for some } m$$

$$1 \qquad T = 0$$

$$\frac{1}{2^n-1} \qquad 0<T< 2^n-1$$

since B_{k+m} has exactly one more -1 than +1 via the transformation of the first property of randomness. Thus, the third property holds true. As a result, the maximal linear sequence is considered a pseudorandom sequence.

In addition, maximal linear sequences have the following interesting properties:

1. Superposition: If initial state A produces sequence S1, and initial state B produces S2, then initial state $A \oplus B$ produces $S1 \oplus S2$

2. Delay-and-add: If $\{A_k\}$ represents the sequence starting at $\{A_k\}$ and $\{A_{k+m}\}$ represents the same sequence delayed by m, there exists n such that $\{A_k\} \oplus \{A_{k+m}\} = \{A_{k+n}\}$

3. Decimation: Sample a sequence every k^{th} bit. If k is even, the resulting sequence is a shifted version of the original; if k is prime, the result is a new maximal length sequence of the same period.

If the initial state is considered the input, and the resulting sequence is considered the output, then the first property is a classic definition of a linear system, hence the name "linear sequence." The second property is important when describing the mathematical properties of linear sequences, since it shows that shifted sequences are members of the same group. The third

property is often used to produce parallel sequences from a single sequence when testing multichannel equipment.

Two characteristics which are also important are the statistical distribution of n-tuple in a sequence generated by an N-stage register and the frequency domain spectrum of the sequence.

a) Statistical Distribution:

Given an N-stage maximal length shift register sequence generator, the examination of one period of 2^N-1 bits using a window of length i which is moved along the sequence in one-bit increments will yield:

i=N All binary combinations of N bits appear exactly once except N zeros, which never appear.

I=N-1 All binary combinations of N-1 bits appear exactly twice except N-1 zeros which appear once.

Etc.

i=N-j All binary combinations of N-j bits appear exactly 2^j times ($0 \leq j \leq N-1$) except N-j zeros which appear 2^j times.

For example, if N=20:

All combinations of 20 bits appear once except 20 zeros.

All combinations of 19 bits appear twice except 19 zeros which appear once.

All combinations of 18 bits appear 4 times except 18 zeros which appear three times.

Etc.

b) Spectral Characteristics:

A periodic pulse is shown in Figure 3. Its power spectral density pulse is shown in Figure 4.

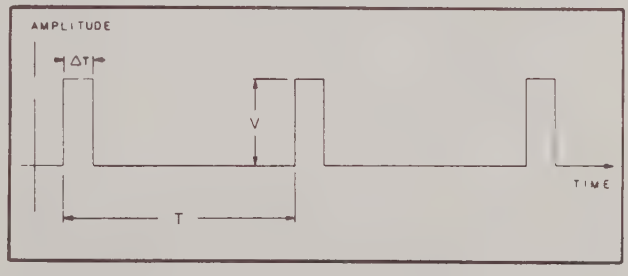

Figure 3. Periodic rectangular pulse train.

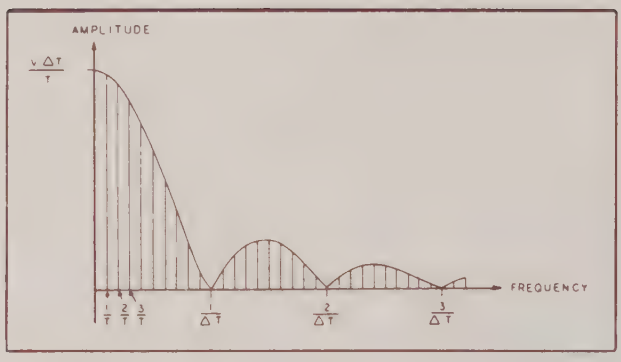

Figure 4. Spectrum of periodic rectangular pulse train.

The following is a summary of the information contained in this spectrum:

a) The fundamental frequency is, by definition, the lowest present in the pulse train, and must therefore be 1/T (where T is the period between pulses).

b) The other components in the diagram must be harmonics of 1/T, that is, 2/T, 3/T, 4/T, etc.

c) The envelope (dotted line) enclosing the components has nulls at frequencies which are multiples of 1/ΔT (i.e., reciprocal of pulse width).

d) The amplitudes of the harmonic components are proportional to the ratio of the pulse width to the pulse period (Δ T/T).

Consider a pseudorandom, maximal linear sequence at frequency fc (Δ T=1/fc).

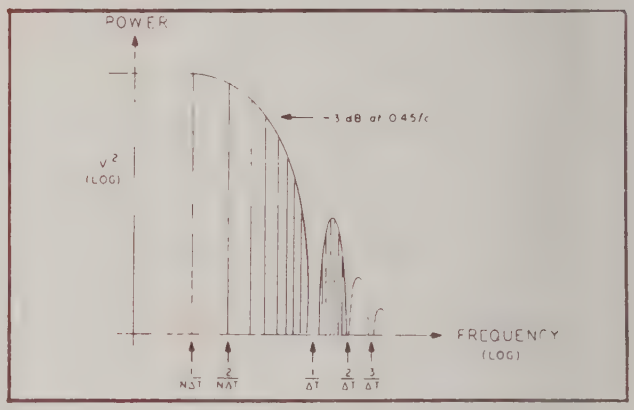

Figure 5. Power spectrum of sequence.

The power spectrum of this periodic binary pattern is similar to that of a rectangular pulse train as shown in Figure 4.

Here, the nulls in the spectrum occur at multiples of the clock frequency, 1ΔT, and the harmonic components are at multiples of the lowest frequency present, 1/T = 1/NΔT, exactly as shown in the pulse train spectrum diagram.

An additional property of maximal linear sequences is that it is possible to generate more than one sequence, which is identical to the original sequence, from the same register, but delayed by a specified number of clock pulses. This is done by using the recurrence relation repetitively as follows:

$$A_n = A_{n-1} \oplus A_{n-3} \oplus A_{n-4} \oplus A_{n-5}$$

$$A_{n+1} = A_{n-1} \oplus A_{n-2} \oplus A_{n-3} \oplus A_{n-4}$$

$$= (A_{n-1} \oplus A_{n-3} \oplus A_{n-4} \oplus A_{n-5}) \oplus A_{n-2} \oplus A_{n-3} \oplus A_{n+4}$$

$$= A_{n-1} \oplus A_{n-2} \oplus A_{n-5}$$

$$A_{n+2} = A_{n+1} \oplus A_{n-1} \oplus A_{n-2} \oplus A_{n-3}$$

$$= (A_{n-1} \oplus A_{n-2} \oplus A_{n-5}) \oplus A_{n-1} \oplus A_{n-2} \oplus A_{n-3}$$

$$= A_{n-3} \oplus A_{n-5}$$

Etc.

Thus, by adding the outputs of the corresponding flip-flops, it is possible to produce parallel sequences, at the time, which are actually delayed versions of the original sequence.

Linear sequences may also be added together to produce longer periods. One method involves adding together the outputs of two or more maximal linear sequences with periods that are prime relative to each other. This method produces non-maximal sequences, which do not have all the properties of maximal sequences, although they do have the first and third properties of randomness.

Still another method is to use the same sequence twice, with the second sequence delayed by exactly one-half of a period. Since the period has an odd length, the clock of the second sequence is off by one-half of a bit. The output is the same maximal linear sequence, but at twice the frequency. Since this can be extended for more than one staggered version, it is thus possible to produce linear maximal sequences at rates greater than 1 GHz.

Non-Linear Sequences

Although there are more non-linear maximal length sequences than linear, little is known about the properties of non-linear sequences except in a few cases. One is developing non-linear sequences from linear ones. For example, add an n-1 input AND gate into the feedback of a maximal linear sequence generator. By selecting the output of the first n-1 flip-flops or their inverses as inputs to the AND gate, it is possible to generate a pseudorandom sequence of any length from 1 to 2^n inclusive, depending on the initial state. Another example involves combining several maximal linear sequences to produce a long non-linear sequence. If S1, S2, and S3 are linear and maximal, then the non-linear sequence produced by S1 $\oplus$ S2 $\oplus$ S3 is easier to synchronize than the same linear sequence, because each of

the three short sequences can be aligned separately. If S1 ⊕ S2 and S3 are correlated with a duplicate S'_1, then

$$C_n = \frac{\text{agreements-disagreements}}{\text{agreements+disagreements}} =$$

0 when S'_1 misalinged
½ when S'_1 aligned

Once S'_1 is aligned, correlating S1 ⊕ S2 and S3 with $S'_1 \oplus S'_2$ produces

C_n = 0 when S'_2 misaligned

½ when S'_2 aligned

and similarly for correlating S1 ⊕ S2 ⊕ S3 with $S'_1 \oplus S'_3$. If P_1, P_2, and P_3 are the lengths of the corresponding sequences, then synchronization will require only $P_1 + P_2 + P_3$ correlations rather than $P_1 P_2 P_3$.

application note

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AN-6
June 1983

AUTOMATIC PROTECTION SWITCH

Protection of digital transmission systems is necessary in the event a working channel experiences such difficulties as an outage due to equipment malfunction, high noise or severe fading. The Automatic Protection Switch (APS) is the most commonly used method of maintaining high system performance protection. It provides this high performance by detecting a degrading system and automatically switching to a spare span line or radio channel. (See Fig. 1.)

In T-carrier applications, the APS at the receiver end provides protection by monitoring several parameters - - BPVs, loss of signal etc. In fact, the manner in which these parameters are used becomes a strong determining factor in realizing the most efficient type of service to be protected.

There are various methods of doing this, but the basic philosophy is the same for most systems. That is, to provide superior performance, the technician must verify that the parameters are correctly set. To do this, two common tests are conducted: (1) verification prior to turn-up for service, and (2) verification during normal traffic conditions. In performing these tests, the Tau-tron S5102 Error Rate Test Set is used. (Refer to Figs. 2 and 3 for proper test setups.)

Not only can the S5102 Error Rate Test Set perform such verification tests, but it can also be used to monitor live traffic. However, in using this test set for such a purpose, the validity of the test becomes questionable. It seems that the S5102 used on live traffic is only valid on the T-span between the APS terminals or the switching sections when the APS terminal is removing BPVs.

Consequently, if technical personnel are monitoring a span line, and one of the switch sections has such a low BPV rate as not to request a switch, then the technician may not be able to see any BPVs at

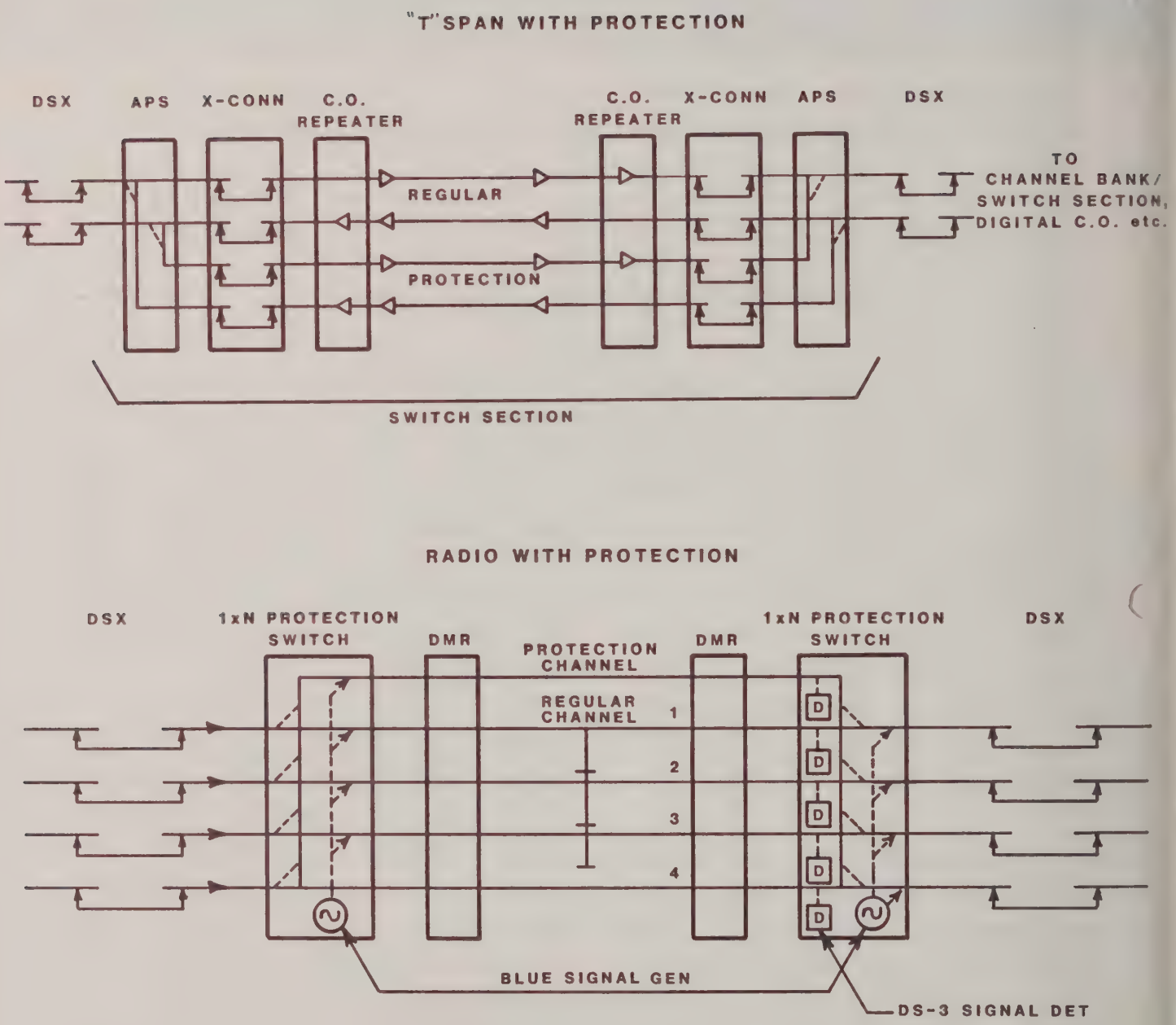

Figure 1 - TYPICAL PROTECTION SYSTEMS

all even though there will be some logic errors present.

This, of course, is the only difficulty encountered in using the S5102 Error Rate Test Set for monitoring system performance on live traffic.

In conclusion, to effectively utilize a typical APS, verification checks must be done periodically. This, thus, preserves the performance of the T-carrier systems.

At the same time, it must be remembered that the APS is not the answer to every system-protection problem, but it is certainly an efficient and reliable method of providing protection for T-carrier systems.

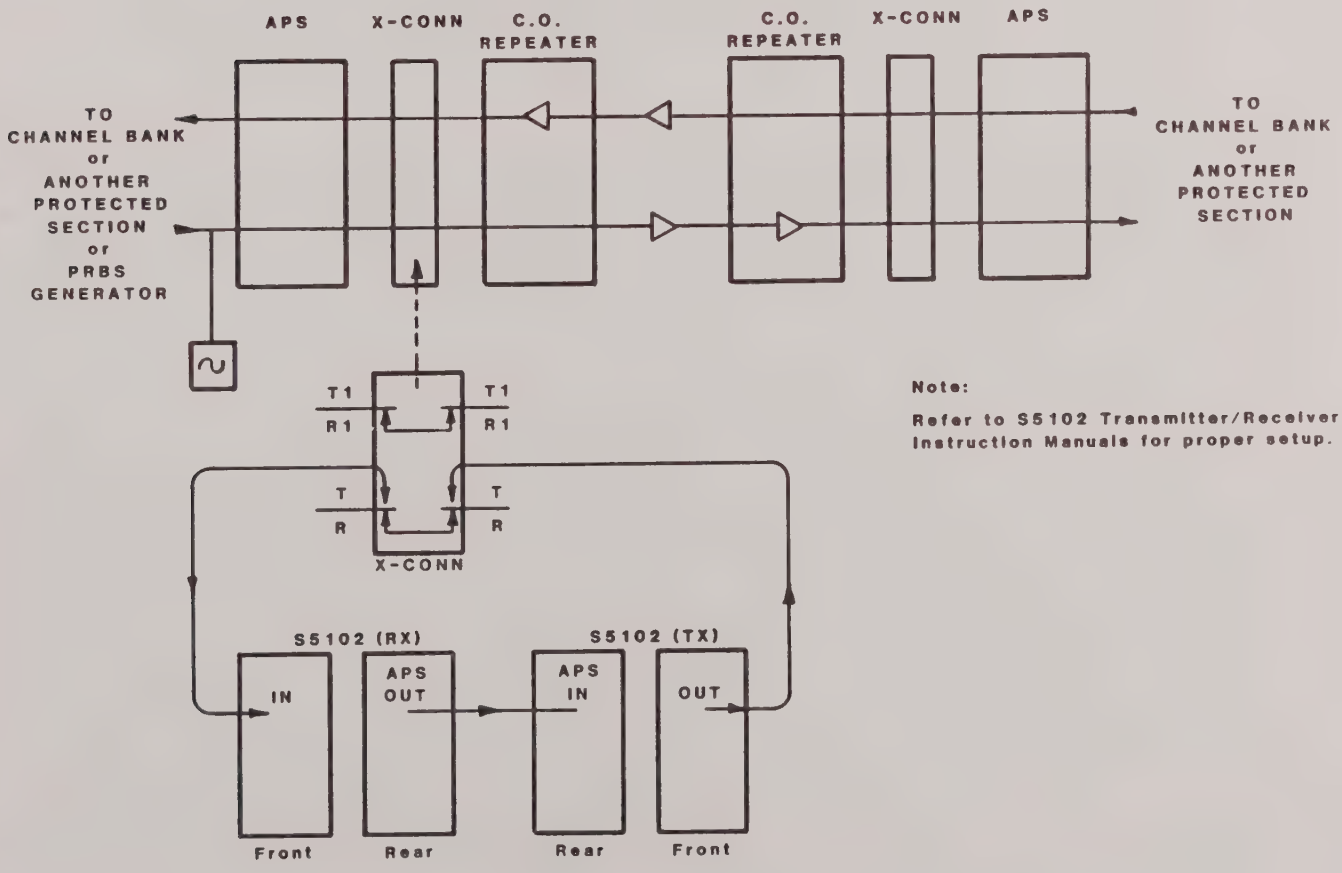

Figure 2 - VERIFICATION PRIOR TO TURN-UP

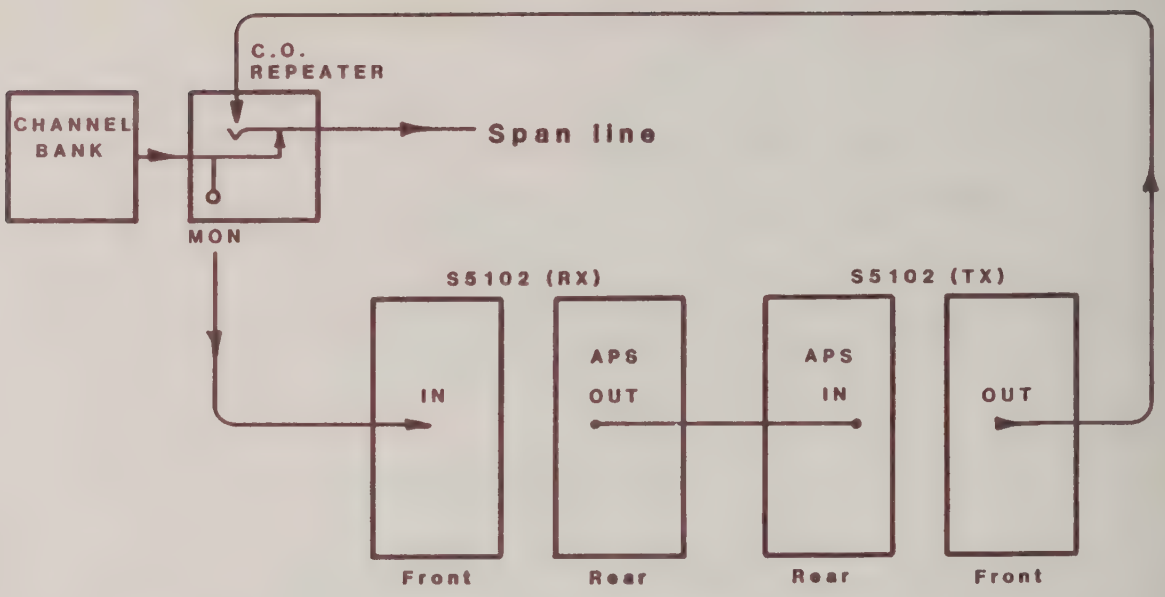

Figure 3 - VERIFICATION DURING NORMAL TRAFFIC

application note

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AN-7
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DS1, DS1C, DS2 AND DS3 ERROR MEASUREMENT AND MONITORING

GENERAL

Two bit-error measurement and monitoring, and two in/out-of-service error recording tests are provided in this Application Note.

S5000-1 DS1 BIT ERROR MEASUREMENT, DMR/FO AGC & ALARM MONITORING

The following procedure is recommended for performing background bit error performance using a T1 line prior to applying traffic to the Digital Microwave Radio (DMR) (refer to Table A and Figure 1). It provides a record of the errors with the time of day to the second, and the AGC voltage and an alarm that has been chosen to be monitored. A threshold can be preset for the AGC voltage to trigger a printout whenever the threshold is exceeded. A record is provided to indicate the number of times the threshold is exceeded during a one second period.

S5000-2 DS1, DS1C OR DS2 BIT ERROR MEASUREMENT, PLUS AGC & ALARM MONITORING

This test configuration allows for the bit error measurement of the DS1, DS1C or DS2 data stream in a loop-back mode over a DMR of infinite length (refer to Table B and Figure 2). The status of the receive signal and the alarm may be recorded at the same time period.

Site "X" is shown in a space density configuration with the DMR "A" channel AGC

being monitored. The receiver alarm circuit is being monitored to indicate when channel "A" switches to channel "B". The S5000 Printing Error Analyzer has the ability to monitor only one DC voltage at a time as shown in the illustration, and will indicate the "A" or "B" radio AGC condition as it exceeds the preset threshold setting in one second. The S5102-TX or RX Error Rate Test Set (Transmitter or Receiver) can be configured to work DS1, DS1C or DS2 (refer to the instruction manual for proper settings). The BIT ERROR output of the S5102 is applied to the S5000 for analyzing.

S5000-3 DS3 OUT-OF-SERVICE, BIT ERROR, AGC & ALARM RECORDING

This test is recommended for measuring the bit errors at a DS3 rate on the DMR (refer to Table C and Figure 3). (CAUTION: This is on an Out-of-Service Test.) The S5200D-TX Digital Transmission Test Set (Transmitter) transmits the DS3 Pseudo-Random Binary-pulse Sequence (PRBS) through the transmission medium. These signals are measured for bit errors at the S5200D-RX (Receiver) and the S5000 reads the AGC voltage and alarms. Since the S5200D and the S5000 operates on a sync-period second principle, there will be a direct correlation as to the errored second, AGC voltage and alarms. All the errors, errored seconds, AGC voltage and alarms will be printed on the S5000 and the bit errors will be printed on the 5901 Printer.

S5000-4 DS3 IN-SERVICE, PARITY ERROR, AGC & ALARM RECORDING

This test is recommended for measuring the parity errors at a DS3 rate on the DMR (refer to Table D and Figure 4). (Note: This is an In-Service Test.) The S5200D-RX is used to measure the parity errors while the S5000 will record the AGC voltage and alarms. Since the S5200D and the S5000 operate on the sync errored second principle, there will be a direct correlation as to the errored second, AGC voltage and alarms. All the errors, errored seconds, AGC voltage and alarms will be printed on the S5000 and the parity errors will be printed on the 5901.

TABLE A
S5000-1

EQUIPMENT REQUIRED FOR TEST
S5000 Printing Error Analyzer

CABLES REQUIRED FOR TEST

CABLE NO.	CONNECTOR	LENGTH
1	T, R & S (310)/T, R, & S	As Required
2	T, R & S (310)/T, R, & S	As Required
3	BNC/BNC	3 Feet
4	BNC/Twin Pin/Clip	As Required
5	BNC/Twin Pin/Clip	As Required

CONNECTIONS

STEP	UNIT	JACK/CONN.	CABLE	UNIT	JACK/CONN.
1	S5000 (R)	DATA-IN	1	T1-Interface	T1, R1 (RCV)
2	S5000 (R)	DATA-OUT	2	T1-Interface	T, R (XMT)
3	S5000 (R)	ANALOG THRESHOLD OUTPUT	3	S5000 (F)	E2
4	S5000 (F)	ANALOG	4	RAD-RCV	AGC/GRD
5	S5000 (F)	E1	5	RAD-RCV	ALM-As Required

SWITCH/CONTROL SETTINGS

STEP	UNIT	SWITCH/CONTROL	SETTINGS	REMARKS
1	S5000 (F)	ERRORS	--	Not Applicable
2	S5000 (F)	E1	TTL	
3	S5000 (F)	E2	TTL	
4	S5000 (F)	ANALOG	± 200V	
5	S5000 (R)	INPUT SLICING LEVEL	ANALOG	Refer to instruction manual for proper setup
6	S5000 (R)	INPUT SLICING LEVEL	NORMAL	Return to NORMAL after Step 5
7	S5000 (R)	BOUNCE PROTECTION-E1	IN	IN-If ALM interface is via relay contacts
8	S5000 (R)	BOUNCE PROTECTION-E2	OUT	OUT-If ALM interface is TTL
9	S5000 (R)	DATA	INTERVAL	T1 PRBS
10	S5000 (R)	PRINTER SQUELCH MODE	As Required	
11	S5000 (F)	PRINT-PERIODIC	As Required	Period Sum Desired

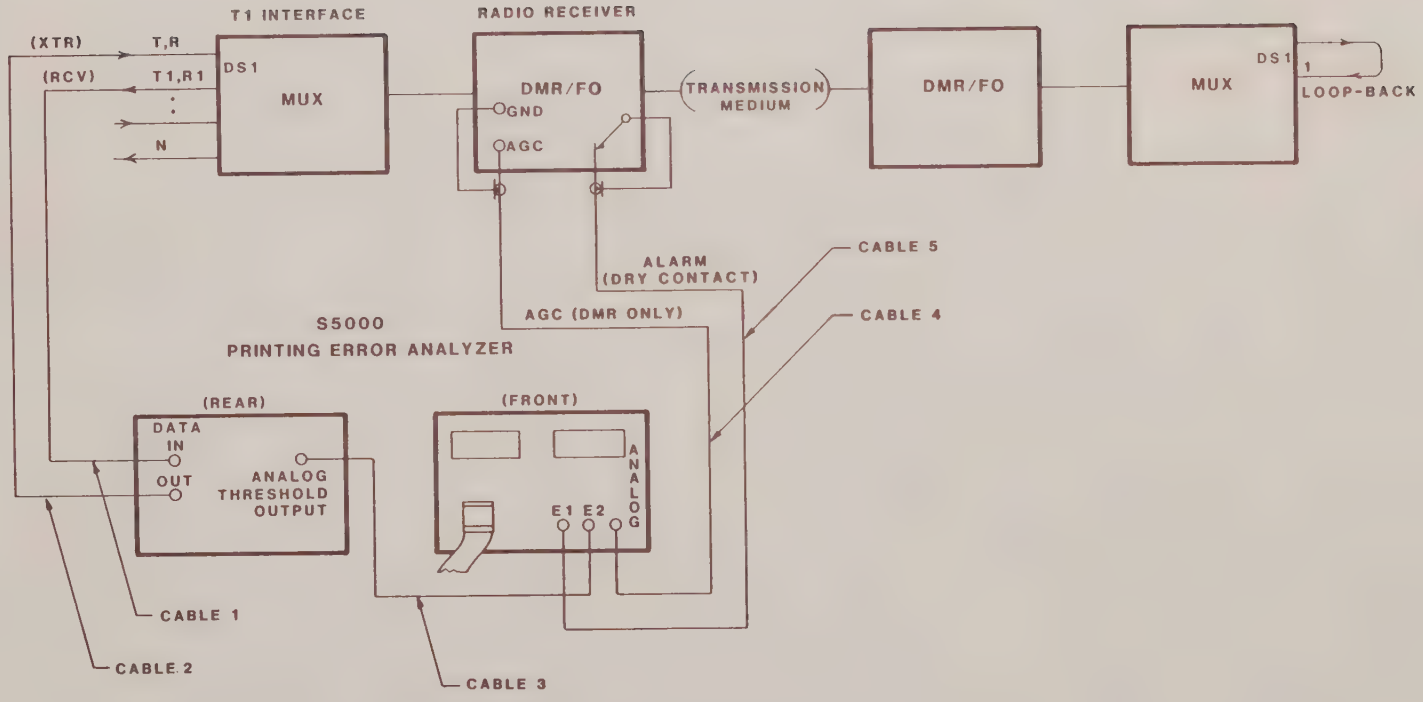

Figure 1 - DS1 BIT ERROR MEASUREMENT, DMR/FO AGC & ALARM MONITORING

TABLE B
S5000-2

EQUIPMENT REQUIRED FOR TEST

S5000 Printing Error Analyzer
S5102-TX Error Rate Test Set
S5102-RX Error Rate Test Set

CABLES REQUIRED FOR TEST

CABLE NO.	CONNECTOR	LENGTH
1	T, R & S (310)/T, R, & S	As Required
2	T, R & S (310)/T, R, & S	As Required
3	BNC/BNC	3 Feet
4	BNC/BNC	3 Feet
5	BNC/Twin Pin/Clip	As Required
6	BNC/Twin Pin/Clip	As Required

CONNECTIONS

STEP	UNIT	JACK/CONN.	CABLE	UNIT	JACK/CONN.
1	S5102-TX(F)	OUTPUT	1	T1-Interface	T & R (XMT)
2	S5102-RX(F)	INPUT	2	T1-Interface	T1 & R1 (RCV)
3	S5102-RX(R)	BIT ERROR	3	S5000 (F)	ERRORS
4	S5000 (F)	E2	4	S5000 (R)	ANALOG THRESHOLD OUTPUT
5	S5000 (F)	E1	5	RAD-RCV A/B	Desired ALM
6	S5000 (F)	ANALOG	6	RAD-RCV A/B	AGC/GRD

SWITCH/CONTROL SETTINGS

STEP	UNIT	SWITCH/CONTROL	SETTINGS	REMARKS
1	S5102 (F)	--	--	Refer to instruction manual for proper setup
2	S5000 (F)	ERRORS	±1V	
3	S5000 (F)	E1	TTL	
4	S5000 (F)	E2	TTL	
5	S5000 (F)	ANALOG	±20V	
6	S5000 (R)	INPUT SLICING LEVEL	ANALOG	Refer to instruction manual for proper setup
7	S5000 (R)	INPUT SLICING LEVEL	NORMAL	Return to NORMAL after Step 6
8	S5000 (R)	BOUNCE PROTECTION-E1	IN	IN-If ALM interface is via relay contacts
9	S5000 (R)	BOUNCE PROTECTION-E2	OUT	OUT-If ALM interface is TTL
10	S5000 (R)	DATA	EXTERNAL	
11	S5000 (R)	PRINTER SEQUENCE MODE	As Required	
12	S5000 (F)	PRINT-PERIODIC	As Required	Period Sum Desired

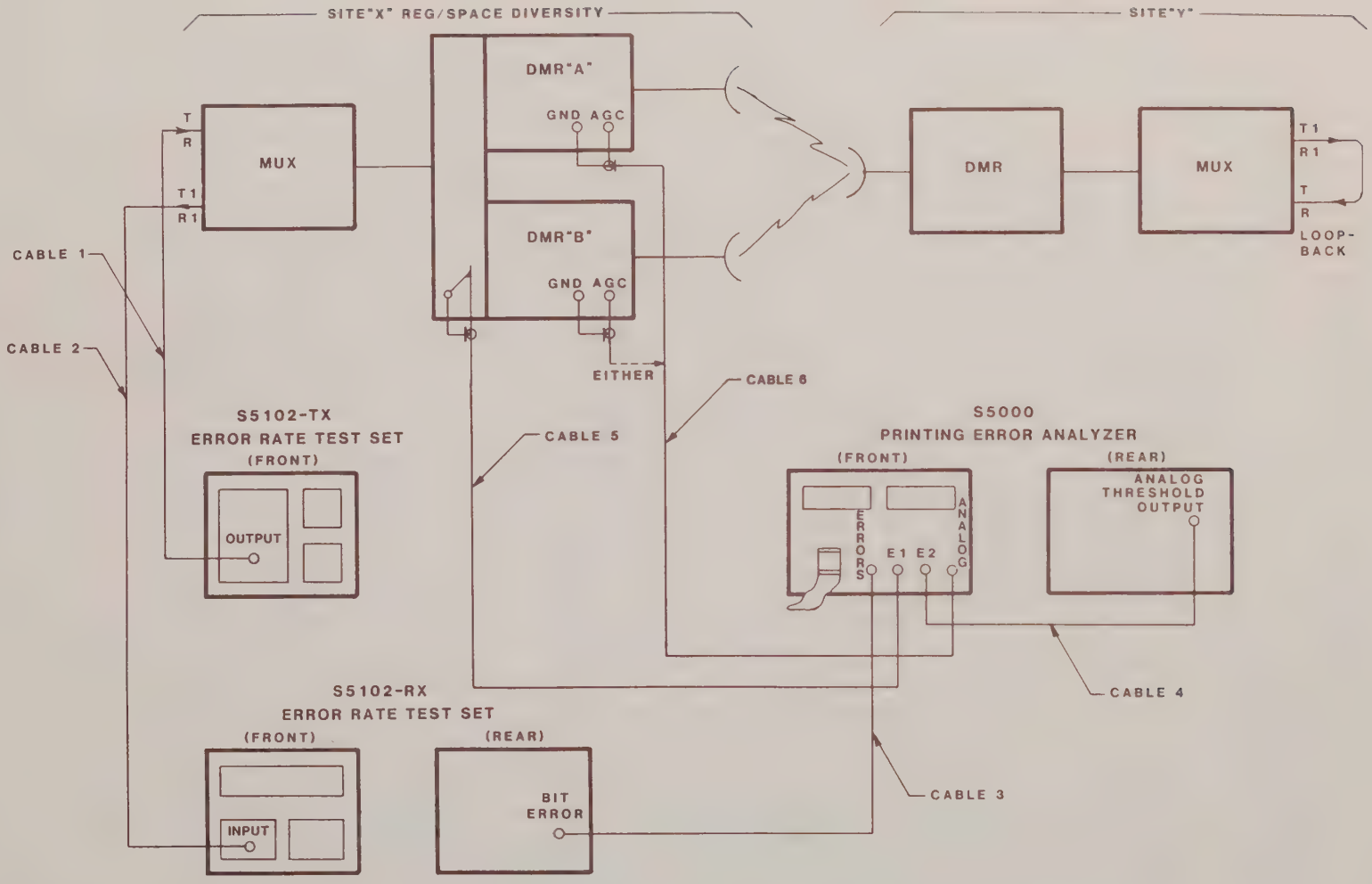

Figure 2 - DS1, DS1C or DS2 BIT ERROR MEASUREMENT, PLUS AGC & ALARM MONITORING

TABLE C
S5000-3

EQUIPMENT REQUIRED FOR TEST

Site A - S5000 Printing Error Analyzer
- S5200D-RX Transmission Test Set
- 5901 Printer

Site B - S5200D-TX Transmission Test Set

CABLES REQUIRED FOR TEST

CABLE NO.	CONNECTOR	LENGTH
Site A - 1	BNC/BNC	6 Feet
Site A - 2	BNC/BNC	3 Feet
Site A - 3	BNC/Twin Pin/Clip	As Required
Site A - 4	BNC/Twin Pin/Clip	As Required
Site A - 5	WECO (358)/As Required	As Required
Site B - 6	WECO (358)/As Required	As Required

CONNECTIONS

STEP	UNIT	JACK/CONN.	CABLE	UNIT	JACK/CONN.
Site A - 1	S5000 (F)	ERRORS	1	S5200D-RX (R)	BIT ERROR
Site A - 2	S5000 (F)	E1	2	S5000 (R)	ANALOG THRESHOLD OUTPUT
Site A - 3	S5000 (F)	E2	3	RAD RCV	ALM-As Required
Site A - 4	S5000 (F)	ANALOG	4	RAD RCV	AGC/GRD
Site A - 5	S5200D-RX (F)	DS3 INPUT	5	RAD RCV	DS3 OUTPUT
Site B - 6	S5200D-TX (F)	DS3 OUTPUT	6	RAD XMT	DS3 INPUT

SWITCH/CONTROL SETTINGS

STEP	UNIT	SWITCH/CONTROL	SETTINGS	REMARKS
Site A - 1	S5200D-RX	--	--	Refer to instruction manual for proper setup
Site A - 2	S5000 (F)	ERRORS	VAR	Refer to instruction manual for proper steup
Site A - 3	S5000 (F)	E1	TTL	
Site A - 4	S5000 (F)	E2	TTL	
Site A - 5	S5000 (F)	ANALOG	±20V	
Site A - 6	S5000 (R)	INPUT SLICING LEVEL	ANALOG	Refer to instruction manual for proper setup
Site A - 7	S5000 (R)	INPUT SLICING LEVEL	NORMAL	Return to NORMAL after Step 6
Site A - 8	S5000 (R)	INPUT SLICING LEVEL	ERROR	If needed, refer to instruction manual for proper setup
Site A - 9	S5000 (R)	BOUNCE PROTECTION-E1	OUT	OUT-If ALM to interface is TTL IN-If ALM interface is relay contacts
Site A - 10	S5000 (R)	BOUNCE PROTECTION-E2	IN	
Site A - 11	S5000 (R)	DATA	EXTERNAL	
Site A - 12	S5000 (R)	PRINTER SQUELCH MODE	As Required	
Site A - 13	S5000 (F)	PRINT-PERIODIC	As Required	Period Sum Desired
Site B - 14	S5200D-TX	--	--	Refer to instruction manual for proper setup

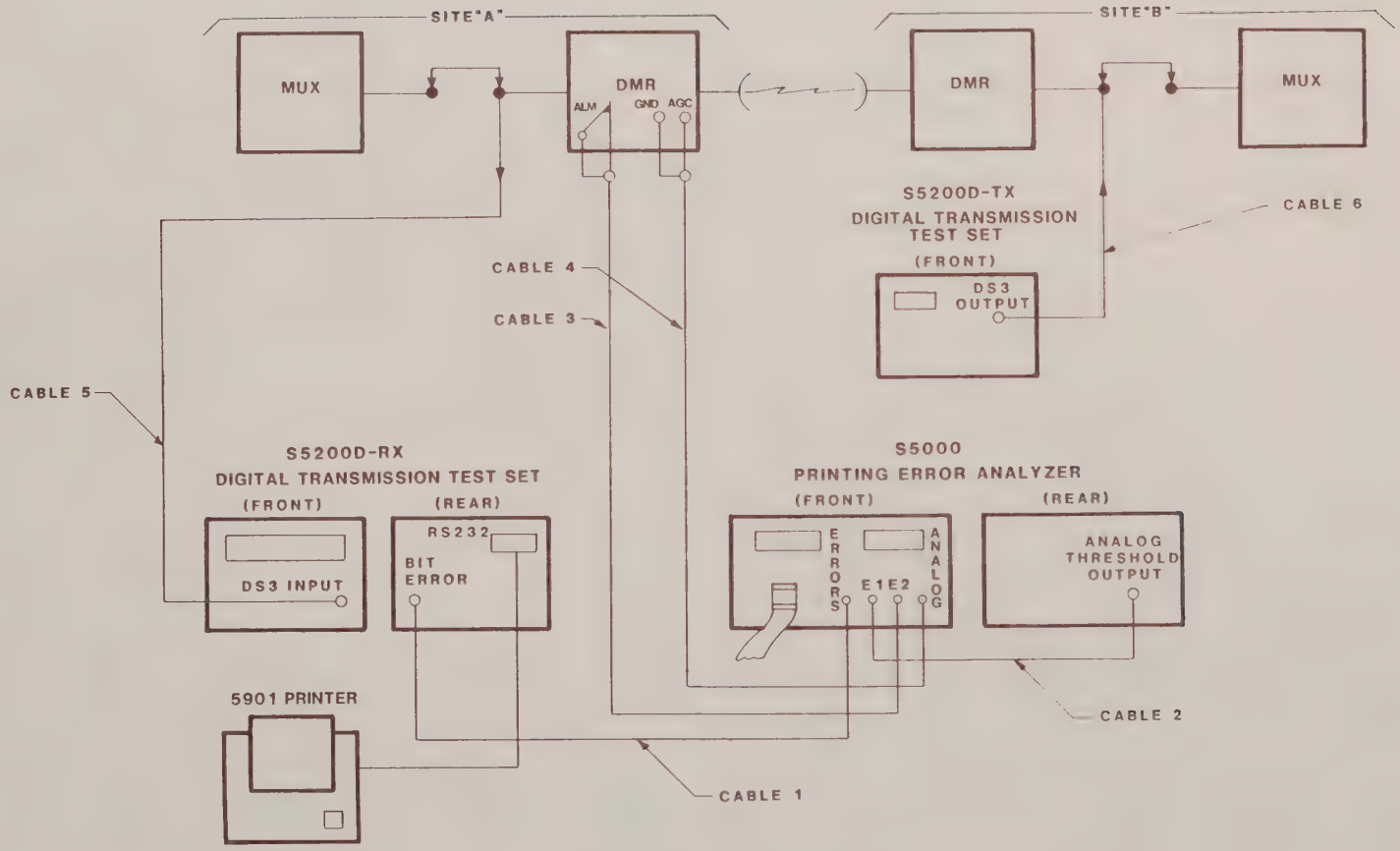

Figure 3 - DS3 OUT-OF-SERVICE, BIT ERROR, AGC & ALARM RECORDING

TABLE D
S5000-4

EQUIPMENT REQUIRED FOR TEST

S5000 Printing Error Analyzer
S5200D-RX Transmission Test Set
5901 Printer

CABLES REQUIRED FOR TEST

CABLE NO.	CONNECTOR	LENGTH
1	BNC/BNC	6 Feet
2	BNC/BNC	3 Feet
3	BNC/Twin Pin/Clip	As Required
4	BNC/Twin Pin/Clip	As Required
5	WECO (358)/As Required	As Required

CONNECTIONS

STEP	UNIT	JACK/CONN.	CABLE	UNIT	JACK/CONN.
1	S5000 (F)	ERRORS	1	S5200D-RX (R)	PARITY ERROR
2	S5000 (F)	E1	2	S5000 (R)	ANALOG THRESHOLD OUTPUT
3	S5000 (F)	E2	3	RAD RCV	ALM-As Required
4	S5000 (F)	ANALOG	4	RAD RCV	AGC/GRD
5	S5200D-RX(F)	DS3 INPUT	5	RAD RCV	DS-3 OUTPUT

SWITCH/CONTROL SETTINGS

STEP	UNIT	SWITCH/CONTROL	SETTINGS	REMARKS
1	S5200D-RX	--	--	Refer to instruction manual for proper setup
2	S5000 (F)	ERRORS	TTL	
3	S5000 (F)	E1	TTL	
4	S5000 (F)	E2	TTL	
5	S5000 (F)	ANALOG	±20V	
6	S5000 (R)	INPUT SLICING LEVEL	ANALOG	Refer to instruction manual for proper setup
7	S5000 (R)	INPUT SLICING LEVEL	NORMAL	Return to NORMAL after Step 6
8	S5000 (R)	BOUNCE PROTECTION-E1	OUT	OUT-If ALM interface is TTL IN-If ALM interface is relay
9	S5000 (R)	BOUNCE PROTECTION-E2	IN	
10	S5000 (R)	DATA	EXTERNAL	
11	S5000 (R)	PRINTER SQUELCH MODE	As Required	
12	S5000 (R)	PRINT-PERIODIC	As Required	Period Sum Desired

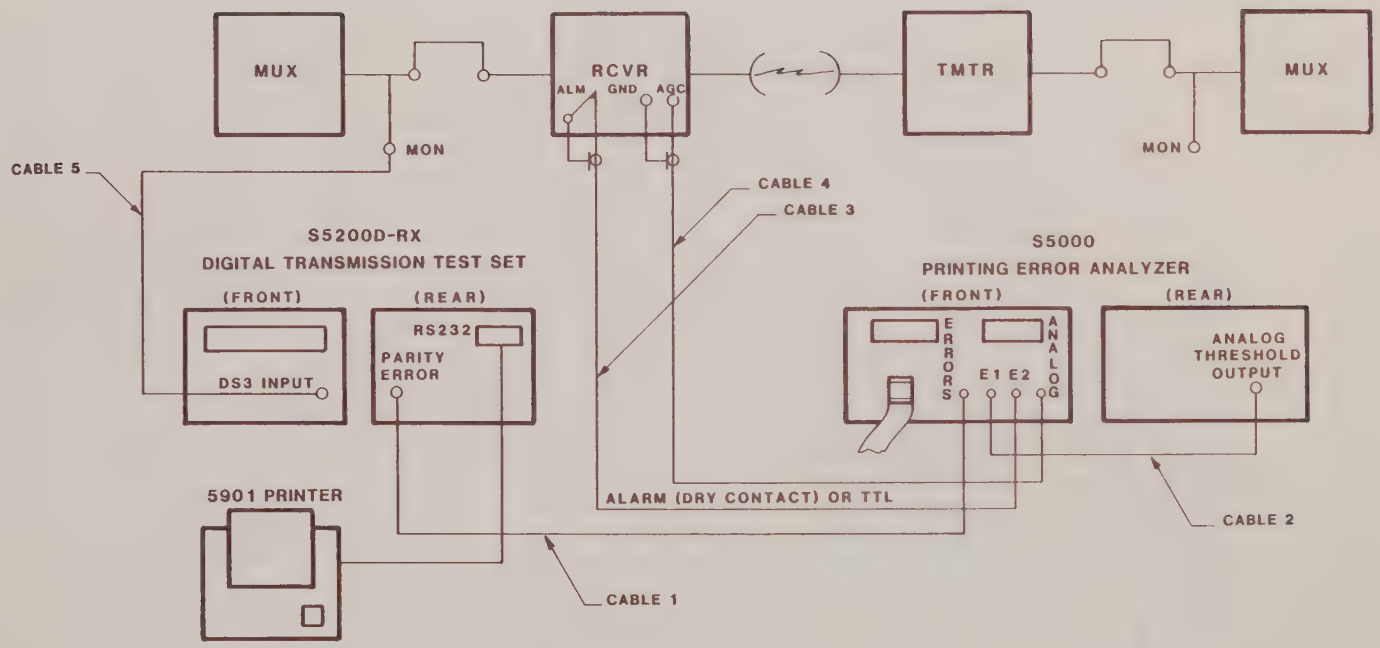

Figure 4 - DS3 IN-SERVICE, PARITY ERROR, AGC & ALARM RECORDING

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AN-8
January 1984

JITTER, WJITS AND DIGITAL TRANSMISSION SYSTEMS

Digital telecommunication networks are expanding and replacing outmoded analog systems, filling most new communication requirements. As more digital system installations increase and interconnect into larger networks, the interest in digital signal jitter increases. To assure that systems can be interconnected without degradation, jitter must be defined and controlled, and system component tolerance to jitter must be known.

This article reviews the sources of jitter in digital transmission systems, and discusses the ability of these systems to tolerate jitter. Parameters necessary to characterize jitter and its effects on system performance are presented including new measurement techniques that provide a simple correlation to system performance.

JITTER PARAMETERS

Jitter on a digital signal can be defined as a dynamic displacement in time of the signal transitions from the ideal. Figure 1A shows an idealized bipolar waveform typical of the T1, T1C, T2, and T3 rate signals used in many digital telecommunication systems. This bipolar-signal represents logic level 1's by positive or negative pulses which usually alternate in polarity; although sometimes purposeful violations in this rule are made. Logic level 0's are transmitted as a zero-volt mid-range level. Figure 1B shows this same waveform with a jitter component. If all of the bipolar pulses in a digital signal were superimposed on one another, similar to an oscilloscope display of random data, the waveform illustrated in Figure 1C would result showing the peak-to-peak amplitude extremes of jitter. Jitter is characterized by the amplitude of these signal transitions, usually expressed in bits or unit interval variations from the ideal and by the frequency content of these displacements.

System components are often designed to tolerate specific levels of jitter over

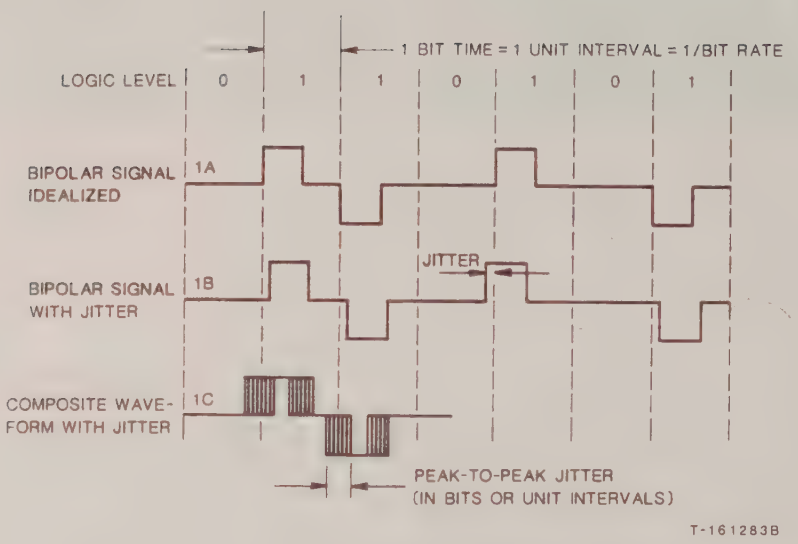


Figure 1. Digital Transmission Jitter

designed frequency ranges and if the jitter on a digital signal exceeds these limits then transmission errors will occur. Recording the jitter amplitude or the instances when jitter exceeds a specific threshold and correlating these to system performance can provide insight into the effects of jitter. It is useful in some applications to consider a frequency weighted jitter measurement since systems typically tolerate more jitter amplitude when the frequency components of the jitter are at low frequencies rather than high frequencies. These tolerance characteristics and the jitter transfer functions of system components are also important parameters that can be a key to error-free performance. These parameters can be determined by generating controlled levels of input jitter at specific frequencies and noting the system's error tolerance limits and by measuring the output jitter versus input jitter.

JITTER SOURCES

A typical digital transmission system is shown in Figure 2, in a one way configuration for simplicity, and consists of:

- a digital multiplexer that combines several input channels into a Time Division Multiplexed (TDM) bit stream;
- a transmitter;
- a transmission medium, such as radio paths, wire or optical cable;
- regenerative repeaters;
- a receiver; and
- terminating equipment such as a demultiplexer, digital switch, or the input to another digital system.

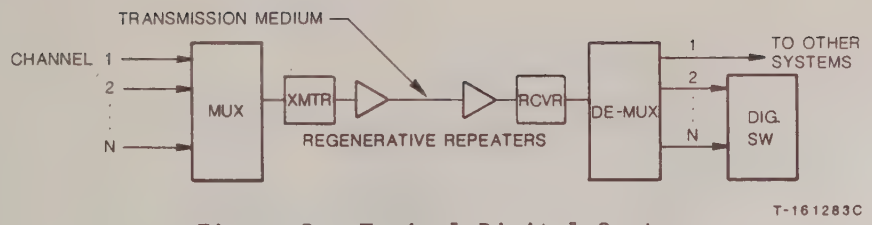


Figure 2. Typical Digital System

Each system component can generate, attenuate, or even amplify signal jitter. In a typical regenerative repeater shown in Figure 3, the digital input signal is amplified then equalized for transmission path distortions, such as the bandwidth rolloff of cables or the dispersive fading of microwave paths. The signal then is sliced at specific decision threshold levels and processed to obtain spectral energy at the digital timing frequency of the input. For bipolar signals, this processing is a full-wave rectification which converts the positive and negative bipolar pulses into a sequence of pulses with the same polarity. These are applied to a narrowband, high Q, bandpass filter, or phase locked loop (PLL), to recover a timing signal which is used to re-time the regenerated output data.

Noise on the low level repeater input or other low level portions of a system from transients, crosstalk and thermal noise, or noise on the decision level points will cause variations in the signal transitions, or noise-like jitter at the repeater output.

The amplitude and frequency response of system timing recovery circuits components can also affect jitter. To a first approximation these circuits will attenuate input jitter frequency components outside their bandwidth and will pass input jitter within their bands. A PLL recovery circuit can even amplify jitter at some frequencies if the loop response is underdamped. The lowpass jitter transfer function of a repeater typically takes the form shown in Figure 4.

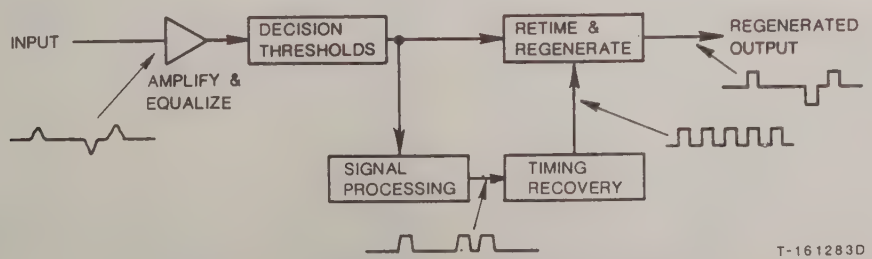


Figure 3. Typical Regenerative Repeater

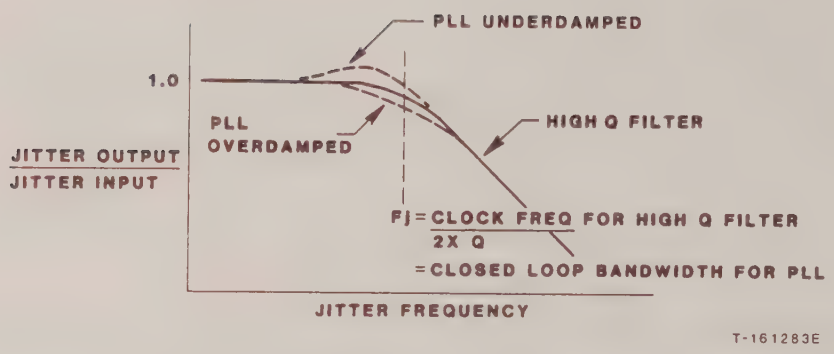


Figure 4. Jitter Transfer Function

Pattern dependent jitter can result from intersymbol interference caused by system response misalignments or when timing recovery circuits are required to process digital signals that contain periods of minimal signal transitions. During the periods the filter output decays and also changes phase if it is not tuned exactly to the input frequency. For the PLL circuit, the output will tend to its free-running frequency during periods of no input which also causes pattern dependent jitter if the free-running and input frequency aren't equal.

Another important source of jitter arises during the multiplexing-demultiplexing process called waiting time jitter. Input channels that are not synchronized to the same clock frequency can be multiplexed together, and one common method used positive justification of the input channels to a common frequency. This method uses pulse stuffing techniques and relies on the fact that the multiplexer output rate is slightly higher than the sum of the individual input channel rates to synchronize the individual channels to the multiplexer aggregate rate by inserting additional pulses in the channel when required. A typical multiplexed digital signal consists of a number of channels that are time division multiplexed together into a single bit stream. Groups of these bits are separated by overhead bits inserted at the multiplexer. These overhead bits serve a number of functions, and the designation of these bits and the design of the overall multiplex bit structure must consider many parameters to assure good overall system performance. Multiplex synchronization time, error tolerance of the framing scheme, requirements for error detection, auxiliary communications channels and the pulse stuffing format, are all important factors.

An example of a common multiplex structure is the 6.312 Mbps T2 format[2] shown in Figure 5. The T2 signal is a result of time division multiplexing, four independent 1.544 Mbps T1 signals. The

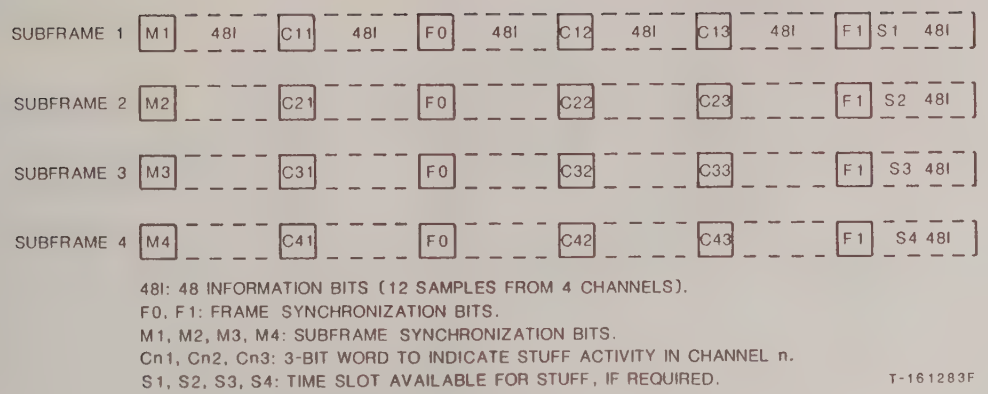


Figure 5. DS2 Frame Format

multiplexer adds overhead bits which are spaced by groups of 12 data bits from each of the four T1 channels. A stuff bit is required occasionally in each channel since the internal multiplexer clock pertaining to each channel is slightly greater than the actual channel rate, and in order to multiplex independent channels into a continuous TDM bit stream this positive justification, or pulse stuffing, technique is used.

For the T2 rate, 48/49 X 6.312 Mbps ÷ 4 or 1545.796 KHz is used for data transmission per nominal 1544 kHz channel. Therefore additional pulses must be added or stuffed by the multiplexer at a nominal 1796 Hz rate. This stuff bit is inserted only at defined times so the stuffing opportunity rate must be at least twice that of the required stuff rate since a stuff may be required yet the opportunity to do so may have just passed. For the T2 signal the nominal justification ratio, or the ratio of the stuff rate to opportunity rate is 1796 Hz:5367 Hz, or about 1:3.

Pulse stuffing is accomplished using elastic stores in which the continuous channel input is written into a buffer, or data store, at the channel rate and read out of the store at the multiplexer channel rate into the TDM bit stream. Phase comparisons between the input and output clocks indicate if a stuff bit is required. The fact that this pulse stuff and its subsequent removal at the demultiplexer can only occur in certain time slots gives rise to the term waiting time jitter. The demultiplexer removes the stuff pulse and uses another elastic store, as in Figure 6, to smooth the one bit phase perturbations that result.

For the T2 example, the stuff bits occur about once for every three stuffing opportunities. At the input to the demultiplexer elastic store, the phase of the data timing advances for three stuff opportunity periods then retards by one bit when the stuff pulse is deleted as illustrated in Figure 7. The elastic store's narrow PLL can smooth

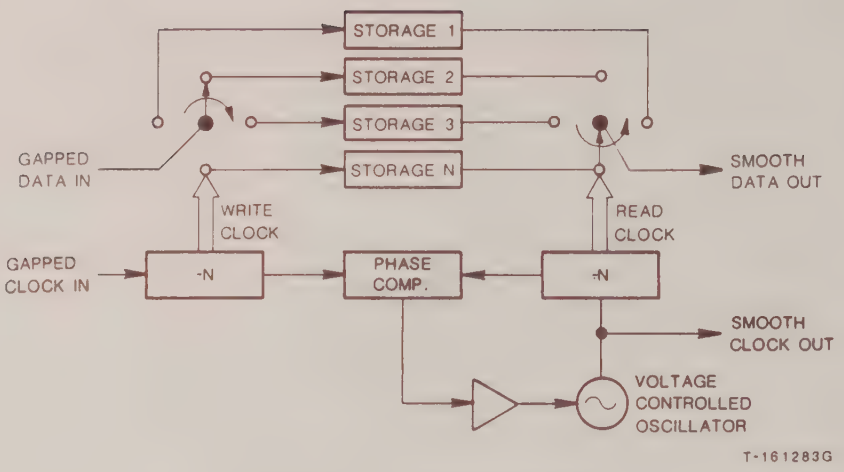


Figure 6. Elastic Store

this one bit, peak-to-peak jitter. However, for real systems this stuffing ratio is not always rational, and frequency components of jitter can extend down to zero frequency. This jitter is usually within the system timing recovery bandwidth and can accumulate with back-to-back demultiplexer-multiplexers.

Other sources of jitter, such as the intrinsic phase noise of oscillators used in the multiplexer clock source and in timing recovery PLL, also add to the overall signal jitter; although these levels are usually low. PLL oscillator noise within the loop bandwidth is filtered, but noise outside the loop band remains and creates some high frequency jitter.

These sources of jitter discussed are important to consider, since they usually occur in various degrees in digital systems and can, in their extreme, cause performance degradations or make connections between systems impossible.

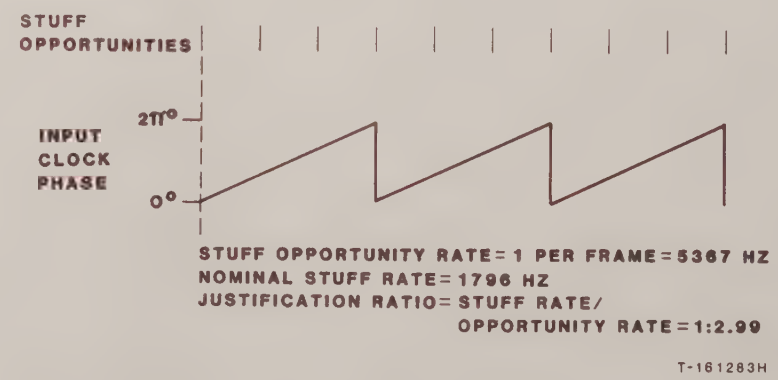


Figure 7. Stuffing Ratio T2 Example

JITTER TOLERANCE

While the sources of jitter previously discussed can be defined and usually controlled by proper system design, the connecting parts of the system must be able to tolerate these jitter levels. More and more specifications are being written that define a particular equipment's tolerance to jitter.

For the regenerative repeater previously discussed the tolerance to input jitter takes the form shown in Figure 8. Frequency components of input jitter greater than the bandwidth of the timing recovery system are not tracked by the PLL and do not pass the fixed filter used in regenerative repeater timing recovery circuits. For this high frequency jitter case, the recovered clock used to retime the data is stationary with respect to the jittering data bit. Thus for a clock that is centered on the data bit, a maximum input jitter amplitude of one-half bit peak or one bit peak-to-peak is allowed for a fullwidth data bit. For bipolar data with halfwidth data bits, this one bit peak-to-peak margin is halved. The recovered clock begins to follow jitter frequencies that are within the timing recovery bandwidth, and the tolerance to jitter increases at a 20 dB (X10) per decade rate for lower jitter frequencies. For a second order PLL, several other lower frequency break points in the jitter tolerance curve may appear. Typically, the first of these is well below 1 Hz and the second is on the order of one-tenth the closed-loop bandwidth for stability reasons.

The jitter tolerance of other components that have filters or PLL timing recovery circuits at their input will have jitter tolerance similar to Figure 8. For equipment that incorporates an elastic

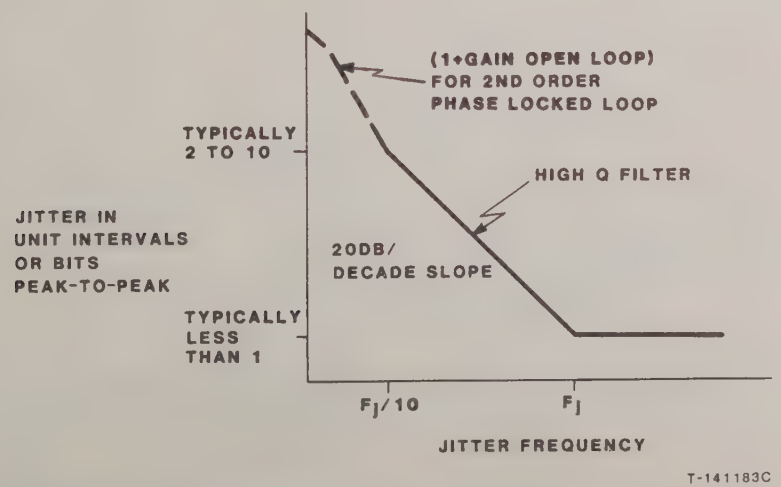


Figure 8. Regenerative Repeater Jitter Tolerance

store for jitter reduction or clock smoothing, such as the demultiplexer previously discussed or as in some digital switches, the jitter tolerance takes a form similar to Figure 9. For this case, the tolerance to input jitter is the lower of the tolerance of a PLL input timing recovery circuit or the tolerance of the very narrow PLL of the elastic store. The tolerance of the elastic store's loop has been increased from one bit peak-to-peak at high jitter frequencies by the addition of dividers in the loop. The dividers permit the PLL phase detector in the elastic store to tolerate greater input phase excursions without losing lock.

JITTER MEASUREMENT

Jitter is present in digital communication systems in varying degrees. How well it is controlled and the ability of the components in a digital system to tolerate it is important to error free performance and to the successful interconnection of digital signals. Both the magnitude and frequency content of jitter are usually important when determining jitter tolerance because of the frequency dependent characteristics of digital equipment.

The exact characterization of jitter in digital communications systems and its effect on performance is often difficult at best, particularly when different digital links made of equipment from different manufacturers are interconnected. In this situation, it is desirable to correlate pertinent jitter measurements with specific performance parameters. Tau-tron has developed the S5104 Digital Transmission Test Set[3] to address measurement needs at the T1, T1C and T2 rates. Jitter generation and jitter measurment capabilities are available in the S5104 which can be

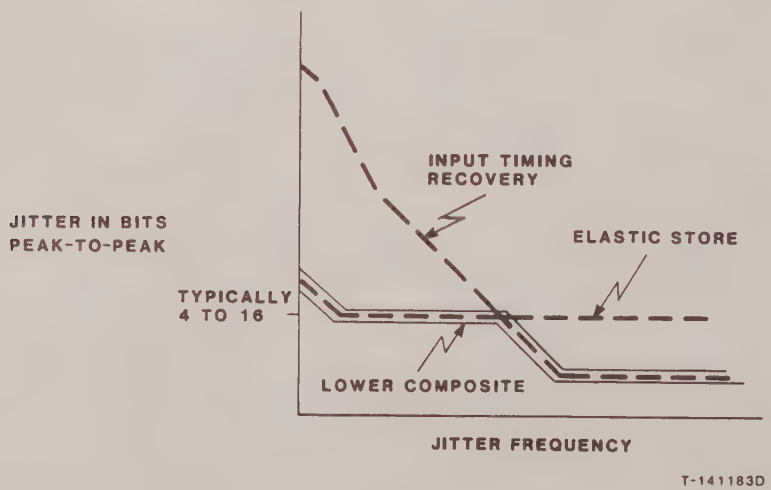


Figure 9. Jitter Tolerance for Equipment with Elastic Store

correlated with other error analysis features of the unit to provide a thorough characterization of the effects of jitter on the performance of digital systems. The following measurements are useful in characterizing jitter and accessing its effects on performance and are provided with simultaneous error measurements in the S5104.

Jitter Tolerance - Both the magnitude and frequency content of jitter are usually important when determining jitter tolerance because of the frequency dependent characteristics of digital equipment. To determine the jitter tolerance of digital transmission equipment, it is required to generate jitter at defined frequencies and increase the jitter amplitude until digital errors are created. The S5104 can apply jitter, as shown in Figure 10, that exceeds CCITT's recommendation 0.171 for equipment of this type. The multiplexing capabilities of the S5104 also permit this jitter tolerance measurement between different rates so a single multiplexer or demultiplexer could be tested, as shown in Figure 11.

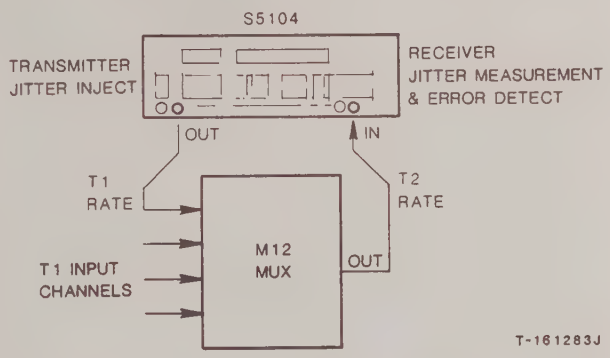
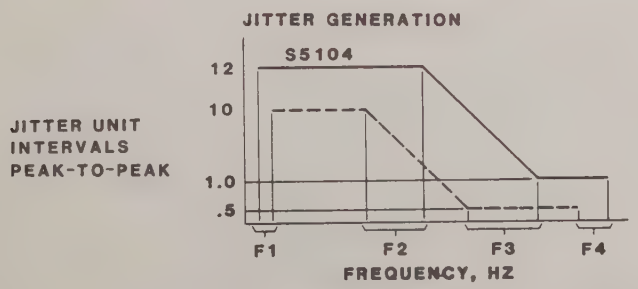


Figure 11. Jitter Tolerance Measurement

Internally generated test patterns with defined jitter applied are used for this test, but a user supplied signal could also be used in the S5104's Thru Mode with controlled jitter and/or errors added to this signal, as shown in Figure 12.

These jitter tolerance measurements are useful in the laboratory to verify a



	F1	F2			F3			F4		
		DS1	DS1C	DS2	DS1	DS1C	DS2	DS1	DS1C	DS2
S5104	1	415	830	1660	5k	10k	20k	50k	100k	200k
CCITT	2	200	-	1600	4k	-	32k	40k	-	160k

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Figure 10. S5104 Jitter Generation

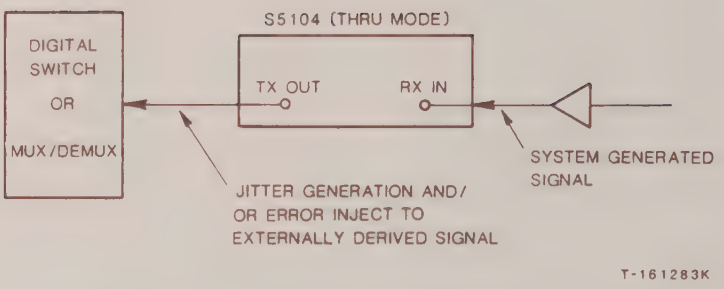
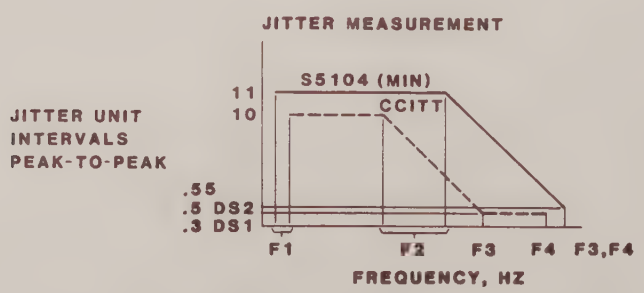


Figure 12. S5104 Thru Mode Application

particular design or to make design trade-off studies. In the factory and field, the jitter generation capabilities of the S5104 are extremely useful for verification of specifications and troubleshooting.

It is often desirable to correlate pertinent jitter measurements with system performance parameters, such as error rate, error seconds or digital synchronization loss. The S5104 provides a powerful jitter characterization capability with the ability to correlate these with system performance. The range over which these jitter measurements are valid exceeds that recommended by CCITT in O.171 for jitter measurement equipment, as shown in Figure 13. The following jitter measurements are made by the S5104 and should prove valuable when characterizing jitter at a particular system point and when correlating the effects of jitter with performance for all T1, T1C and T2 systems.

Jitter Magnitude - A measurement of peak-to-peak jitter is useful at the input to equipment, such as demultiplexers and digital switches, that have a jitter tolerance that is flat over a broad frequency range as in Figure 9.



	F1			F2			F3			F4		
	DS1	DS1C	DS2	DS1	DS1C	DS2	DS1	DS1C	DS2	DS1	DS1C	DS2
S5104	2	4	8	2.5k	5k	10k	50k	100k	200k	50k	100k	200k
CCITT	10	-	10	200	-	1600	7k	-	32k	40k	-	160k

T-161283L

Figure 13. S5104 Jitter Measurement

Correlating this with system performance could help in diagnosing jitter related problems.

Maximum Jitter - A stored measurement of the maximum peak-to-peak jitter, that occurs during a particular measurement period, serves to verify the extremes of jitter excursions on a digital signal. The limits of these measurements to assure application to most systems is also specified in CCITT Recommendations O.171.

Jitter Threshold Seconds - The number of seconds during which the peak-to-peak jitter exceeds a user selected threshold is recorded. This measurement is useful in characterizing the jitter on a system with the threshold set relative to a particular system tolerance level.

Weighted Jitter Measurements (wjits) - Longer digital systems that are interconnected through repeaters are common. The tolerance of a repeater input to jitter amplitude excursions is a function of frequency, as in Figure 8, and trying to correlate absolute jitter with system performance may prove frustrating since the frequency of the jitter may not be known. A new measurement termed "wjits" which is a frequency weighted jitter measurement is proposed which represents a single numerical representation of jitter magnitude that is proportional to the jitter's detrimental effect on the system regardless of the frequency content of the jitter. The weighting curve has a high-pass response, as shown in Figure 14, which complements the jitter tolerance curve of Figure 8.

The frequency break point of the curve, corresponds to that in the jitter generation curve of CCITT Recommendation O.171 and the frequency where absolute jitter and wjits are equal, is equal to Bit Rate/1000 to simplify interpretation

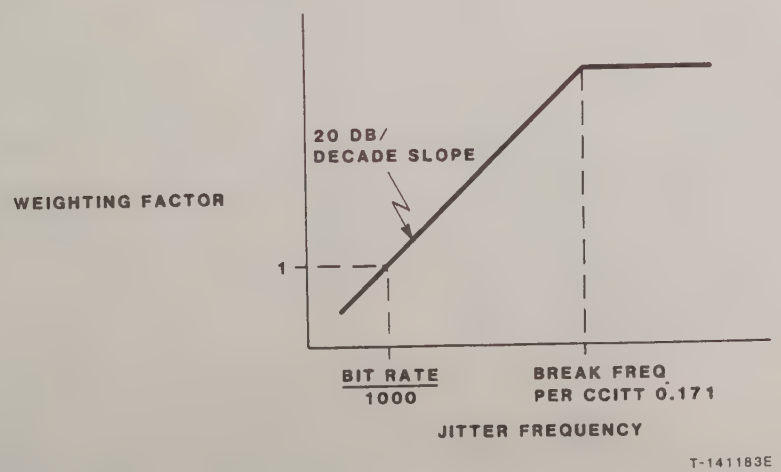


Figure 14. WJIT Measurement Jitter Weighting Factor

of the results. Wjits should provide a simple measurement of the signal jitter which has a direct relationship to system performance.

As an example, consider a 6.312 Mb/s T2 system that has a repeater with a typical tolerance to jitter that decreases with increasing frequency with a tolerance to jitter at 6.312 MHz - 1000, or 6.3 kHz, of 3-bits peak-to-peak. These parameters could be verified with the S5104 or determined from equipment specifications. If a weighted jitter measurement at this system location ever approached 3 wjits, then the system would be close to an error condition regardless of the frequency content of the jitter. System locations could be measured during normal maintenance procedures or when trouble is indicated to obtain a simple measurement of the signal jitter which has a direct relationship to system performance.

SUMMARY

Jitter is a parameter of interest, as more and more digital communication systems are installed and interconnected. Defining and controlling jitter can be critical to successful system interconnects and error free network performance.

A typical digital transmission network consists of multiplexers, demultiplexers, transmitters, receivers, regenerative repeaters, and switches. Common sources of jitter are found to be intrinsic jitter from oscillator noise, pattern dependent jitter magnified by system distortions and intersymbol interference effects, noise-like disturbances on signals from such perturbations as crosstalk and power transients, and waiting time jitter in the multiplexing process. Jitter has dynamic components of amplitude and frequency which can be modified by the components in a system. Characterization of jitter and effects on performance is useful to development engineers, factory test personnel, and field craftsmen. Several measurement parameters including peak-to-peak jitter measurements, maximum system jitter and jitter threshold seconds are useful when correlated with system performance. Some new measurement parameters which weight the effects of both magnitude and frequency components of jitter can be more useful than conventional measurements in some instances. These frequency weighted jitter measurements, termed wjits, provide a simple, numerical representation of digital signal jitter proportional to its detrimental effects on system performance.

Tau-tron's S5104 Digital Transmission Test Set offers all of these jitter measurements and jitter generation correlated to system performance para-

meters. These measurements are provided at and between the T1, T1C and T2 transmission rates through the multiplexing-demultiplexing features of the S5104, and offer the user unparalleled digital system characterization and diagnosis capabilities in a single, portable unit.

References:

1. Transmission Systems for Communications, Revised Fourth Edition December 1971, Chapter 26, Bell Telephone Laboratories, Inc.

2. The M12 Multiplex Compatibility Specification, AT&T Compatibility Bulletin, CB128, Octorber 5, 1979.

3. S5104 DS1/DS1C/DS2 Digital Transmission Test Set Specification, Tau-tron Form 0294-0083A.

NOTES

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